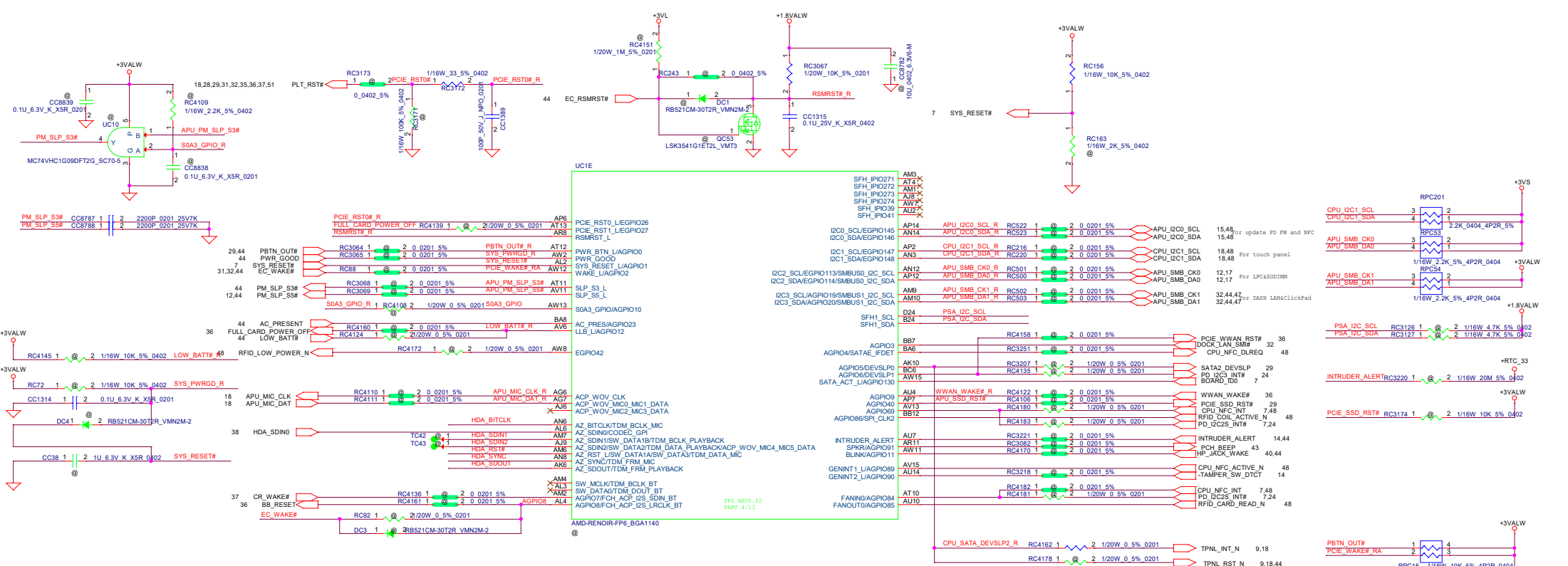
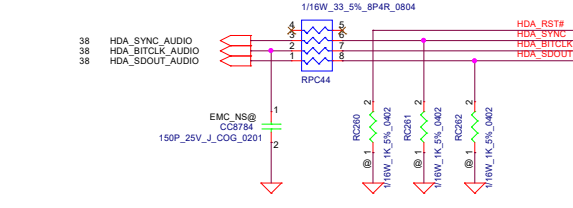
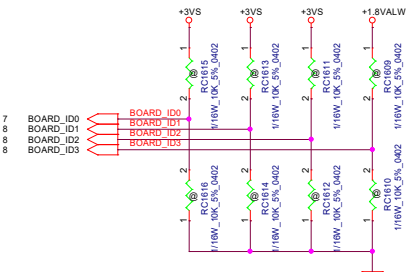


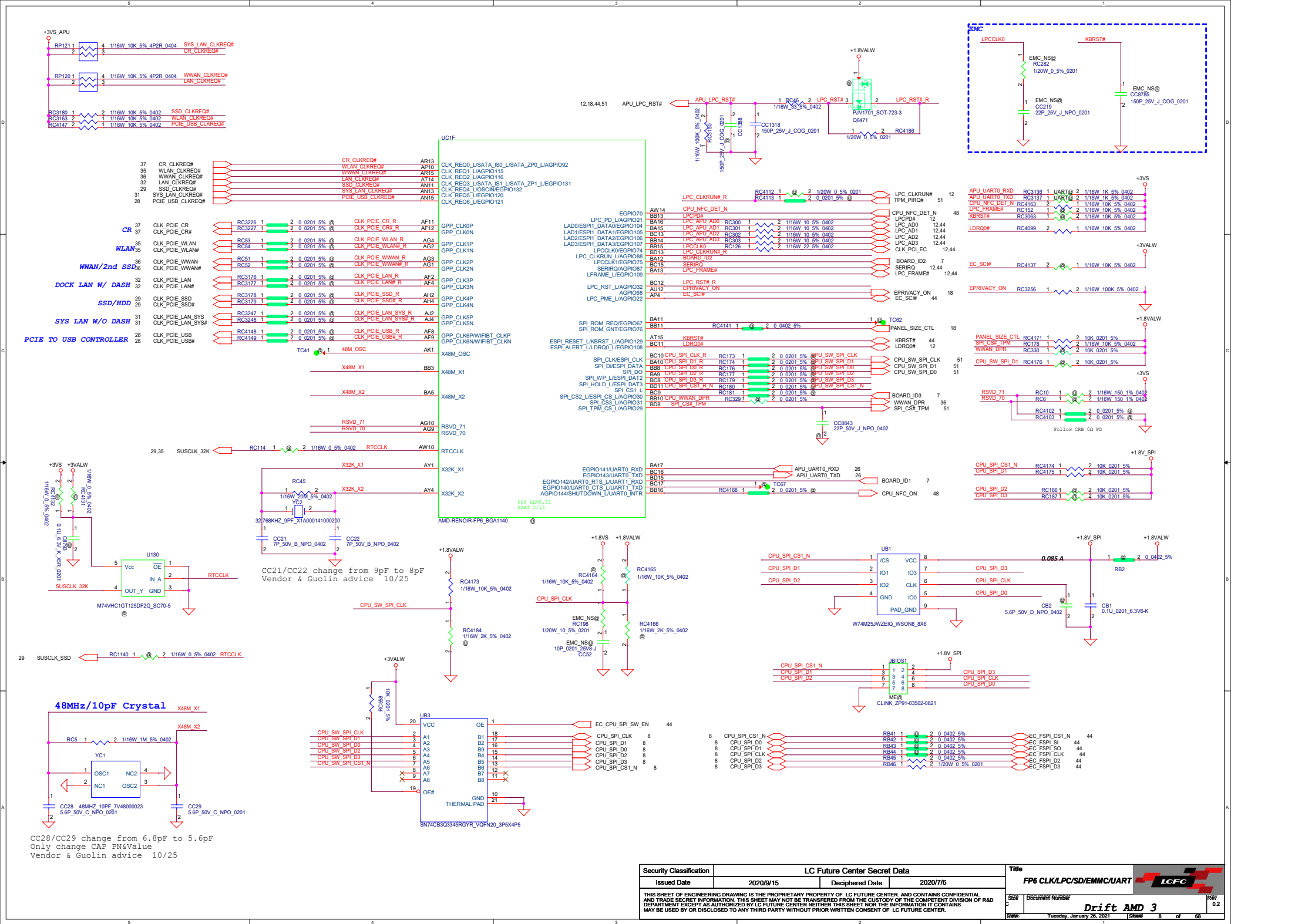
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| Date: Tuesday, January 26, 2021 | | Sheet: 3 | | of 68 | |




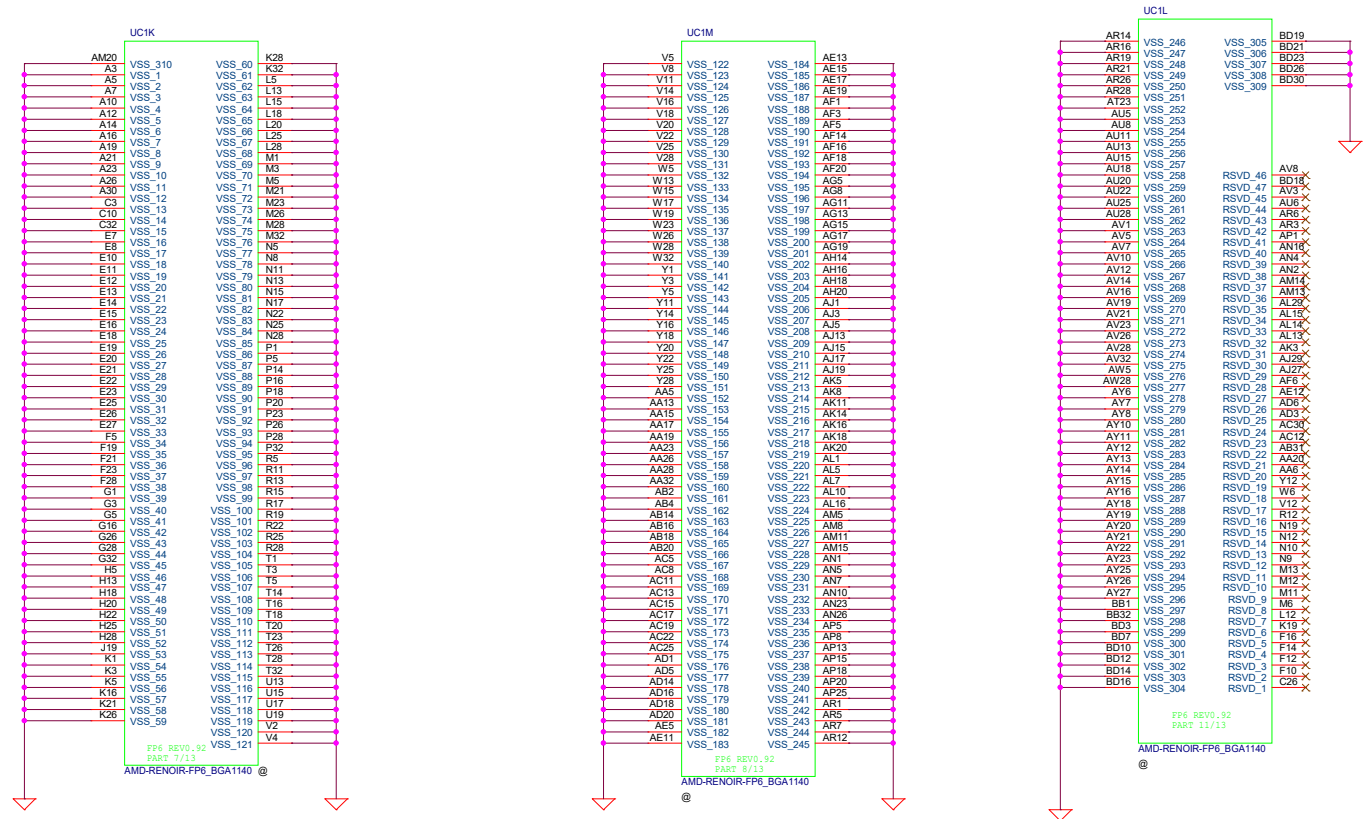
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| Date | Tuesday, January 26, 2021 | Sheet | 7 | of 68 |

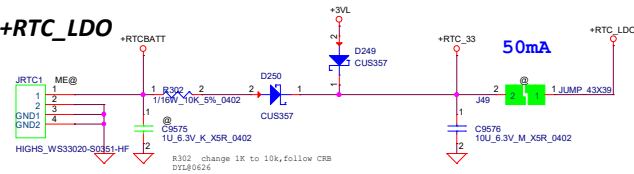


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| | | | | Date: Tuesday, January 26, 2021 | | Sheet 8 of 68 | |

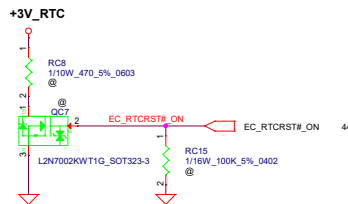


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| Date: | Tuesday, January 26, 2021 | | Sheet | 11 | of 68 |

+RTC_LDO

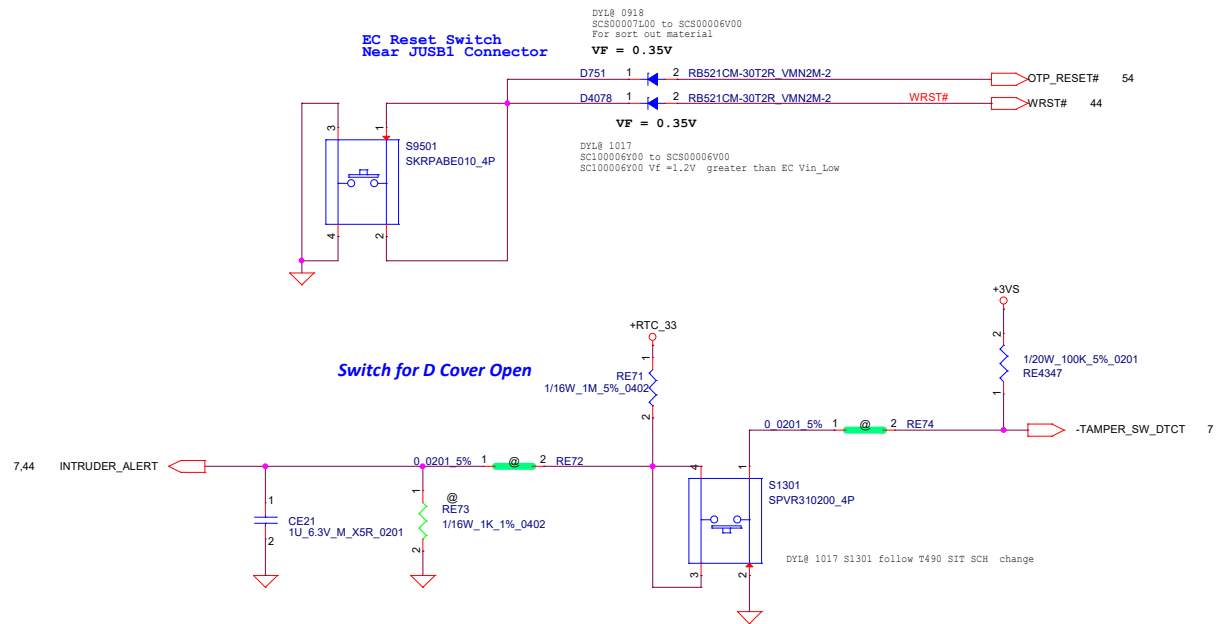



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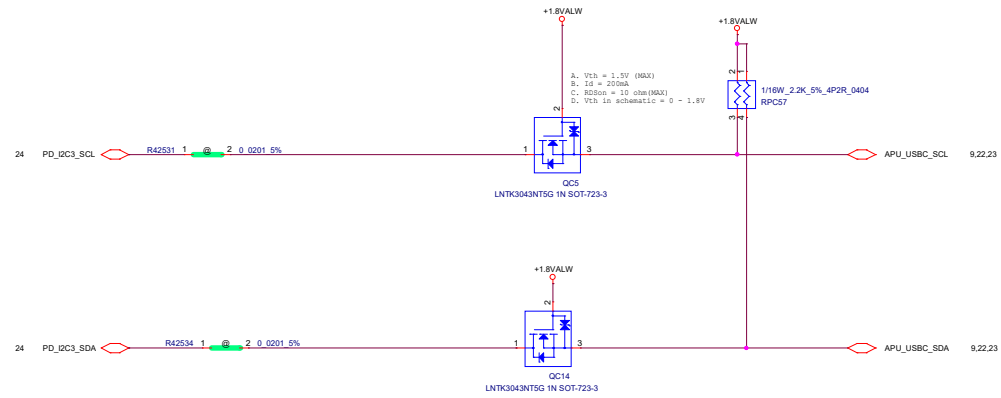
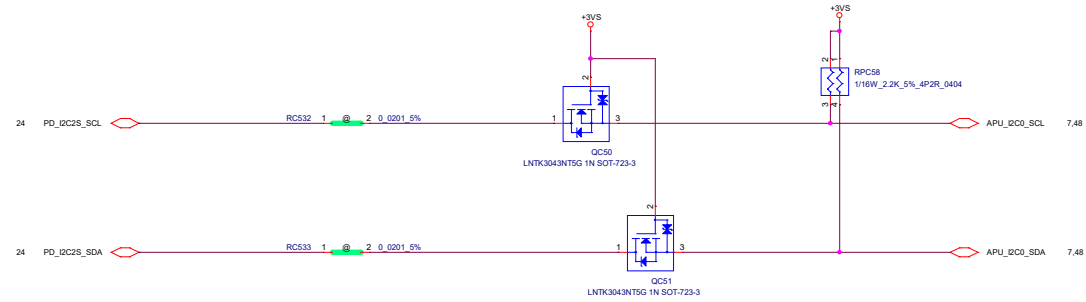


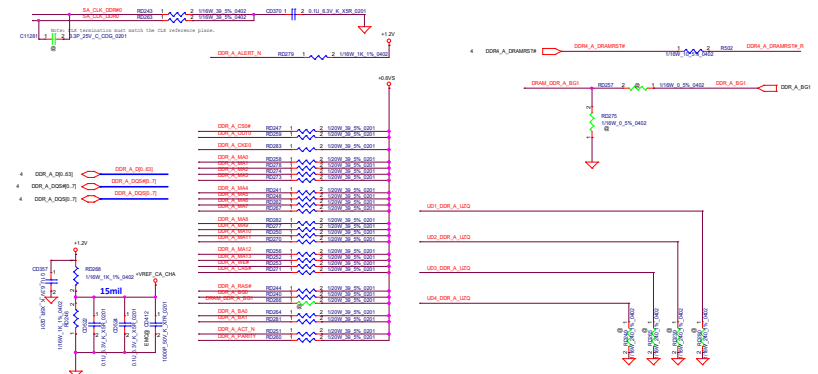
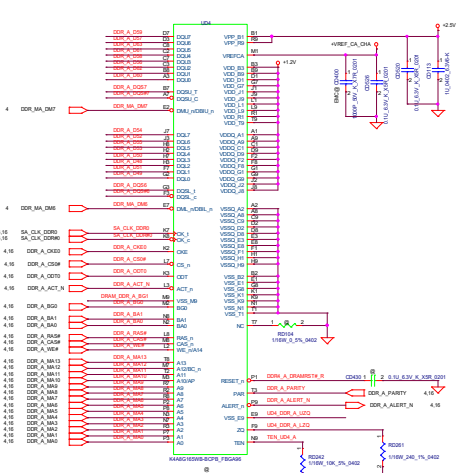
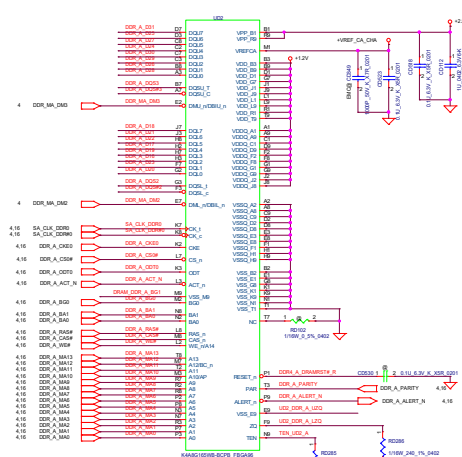
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| 2020/8/15 | | 2020/7/6 | | Document Number | |
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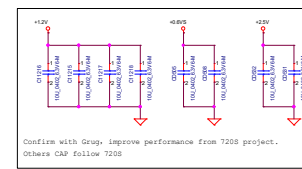


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| Custom | | | | | | 0.2 |
| Date: | | Tuesday, January 26, 2021 | | Sheet | 14 of 68 | |

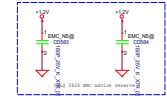




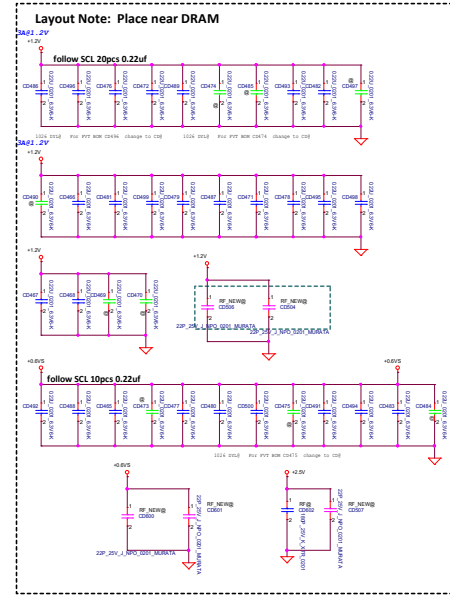
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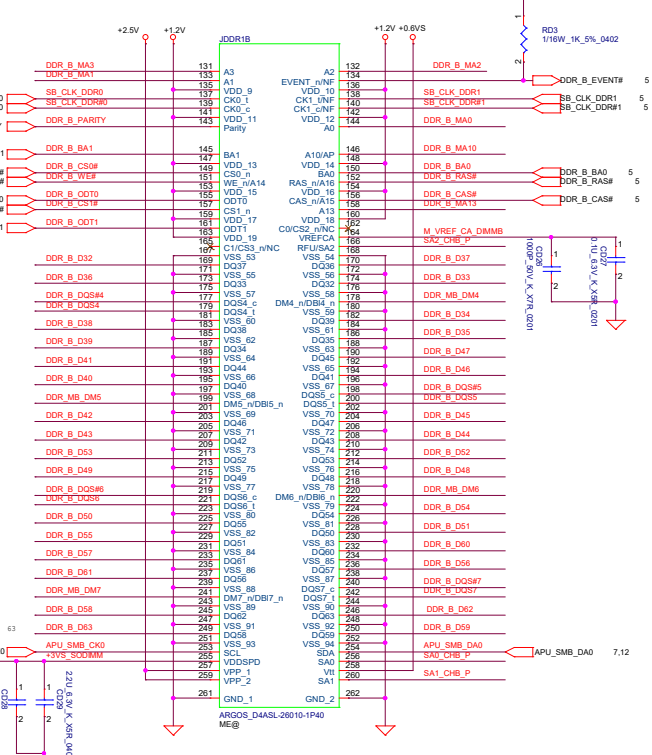
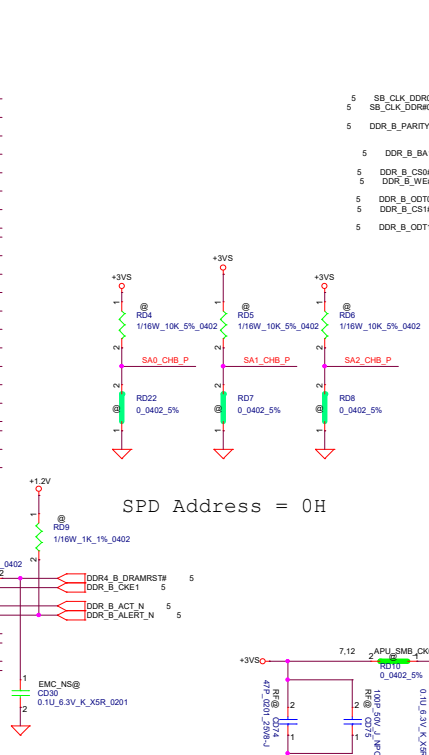
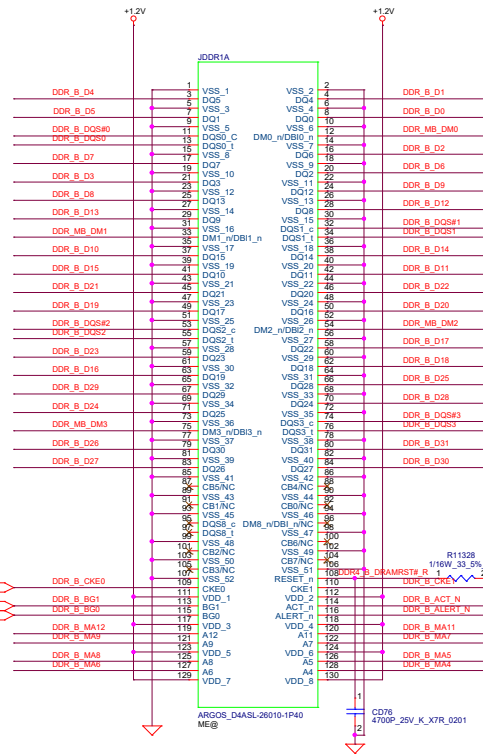
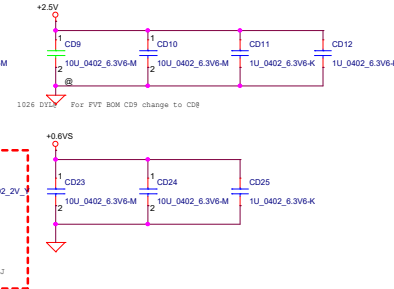
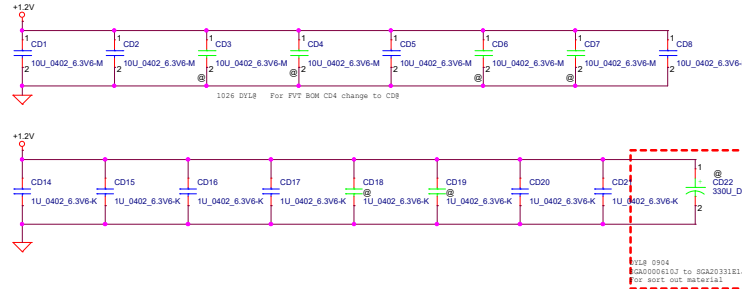
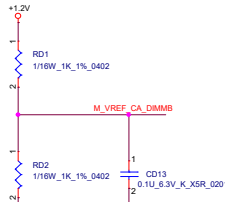
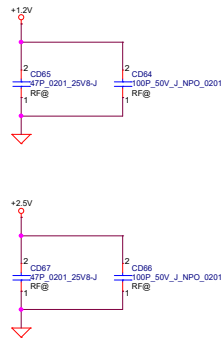


Confirm with Grug, improve performance from 720S project.
Return 312, follow 720S

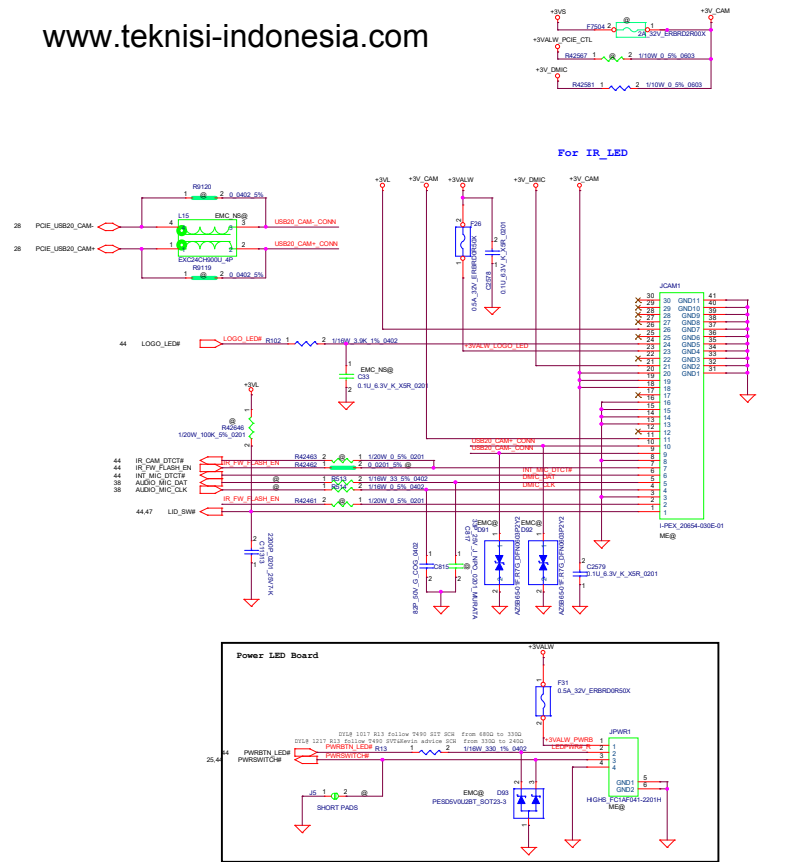
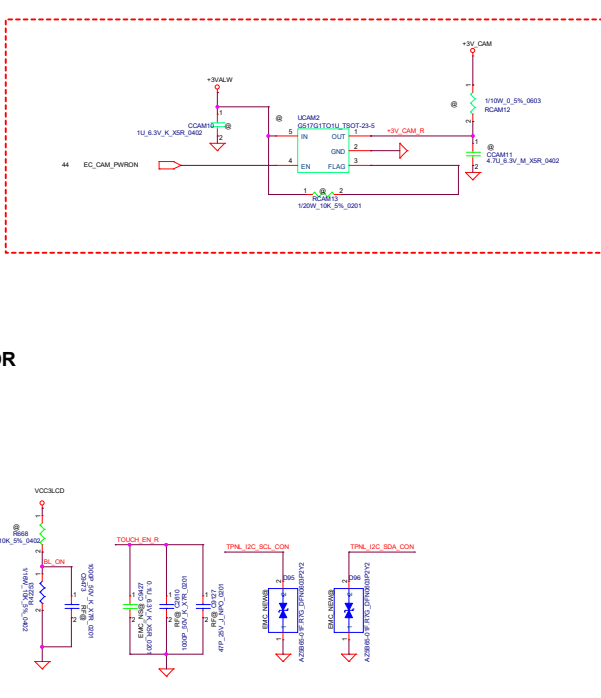
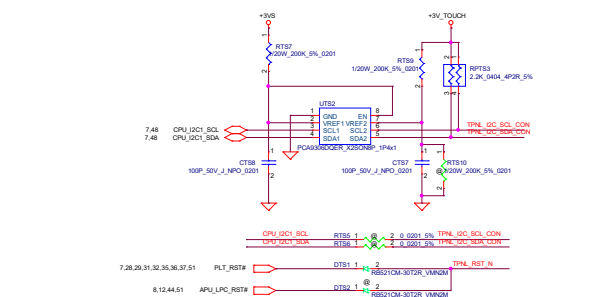
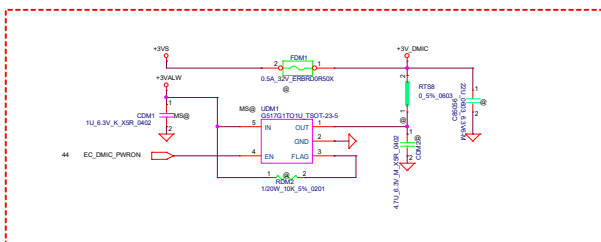



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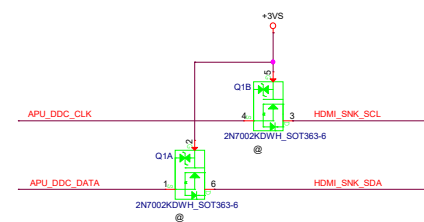
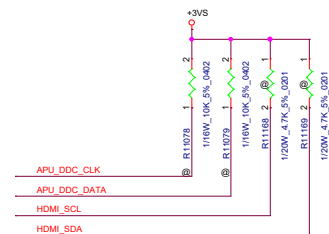
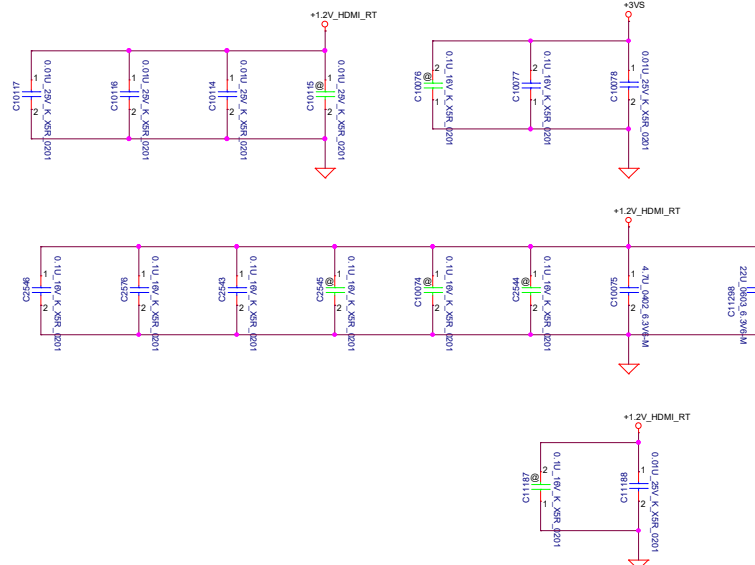





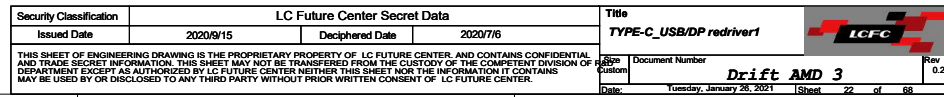
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| D03 | DDR_B_D0 | D0-D7 | D035 | DDR_B_D03 | D32-D39 |
| D04 | DDR_B_D0 | D0-D7 | D036 | DDR_B_D03 | D32-D39 |
| D05 | DDR_B_D0 | D0-D7 | D037 | DDR_B_D03 | D32-D39 |
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| D08 | DDR_B_D0 | D0-D7 | D040 | DDR_B_D03 | D32-D39 |
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| D14 | DDR_B_D0 | D0-D7 | D046 | DDR_B_D03 | D32-D39 |
| D15 | DDR_B_D0 | D0-D7 | D047 | DDR_B_D03 | D32-D39 |
| D16 | DDR_B_D0 | D0-D7 | D048 | DDR_B_D03 | D32-D39 |
| D17 | DDR_B_D0 | D0-D7 | D049 | DDR_B_D03 | D32-D39 |
| D18 | DDR_B_D0 | D0-D7 | D050 | DDR_B_D03 | D32-D39 |
| D19 | DDR_B_D0 | D0-D7 | D051 | DDR_B_D03 | D32-D39 |
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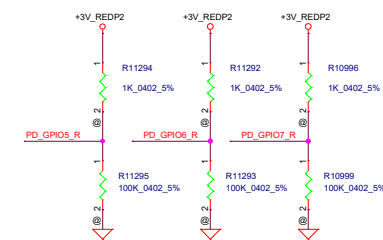


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| | | | | Rev. 02 |

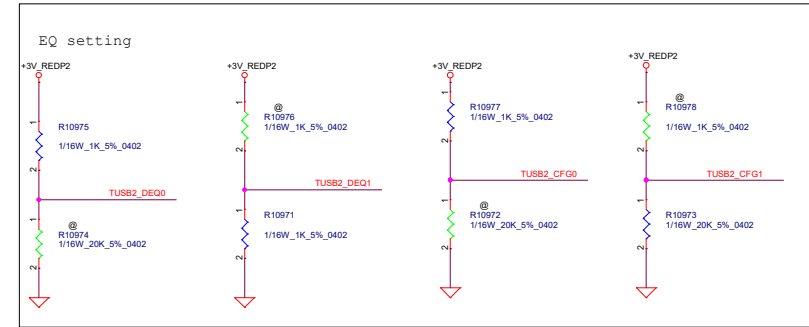



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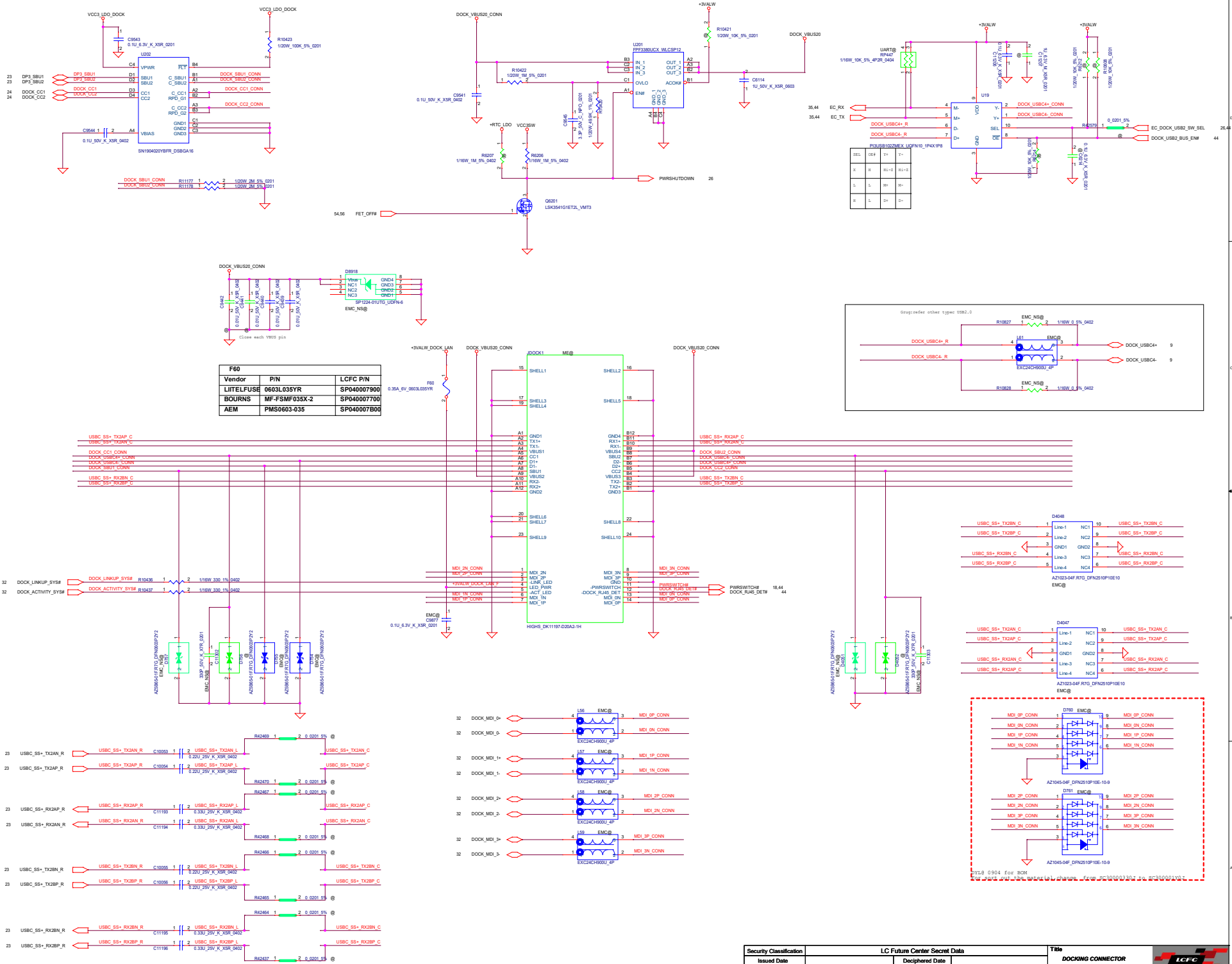


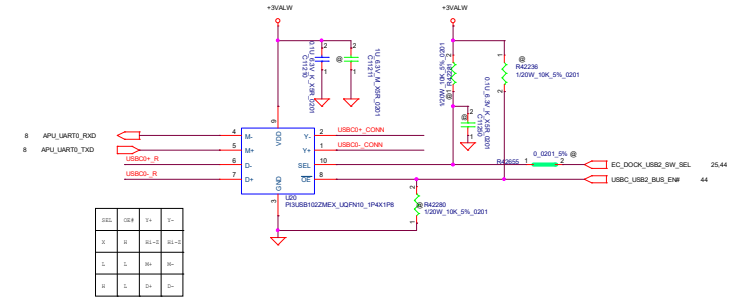
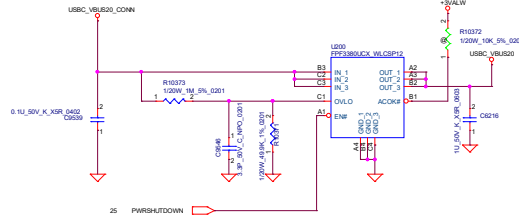
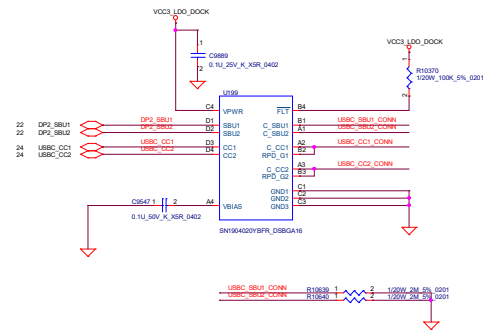


The schematic shows two signal paths for USB2_VBUS and USB2_DIR1. Both signals are connected to a 3V_RED P2 pin. The USB2_VBUS path includes a 10k resistor (R10995) and a 1/16W 1k 5% 0402 resistor (R10962) to ground. The USB2_DIR1 path includes a 10k resistor (R10994) and a 1/16W 1k 5% 0402 resistor (R10963) to ground.

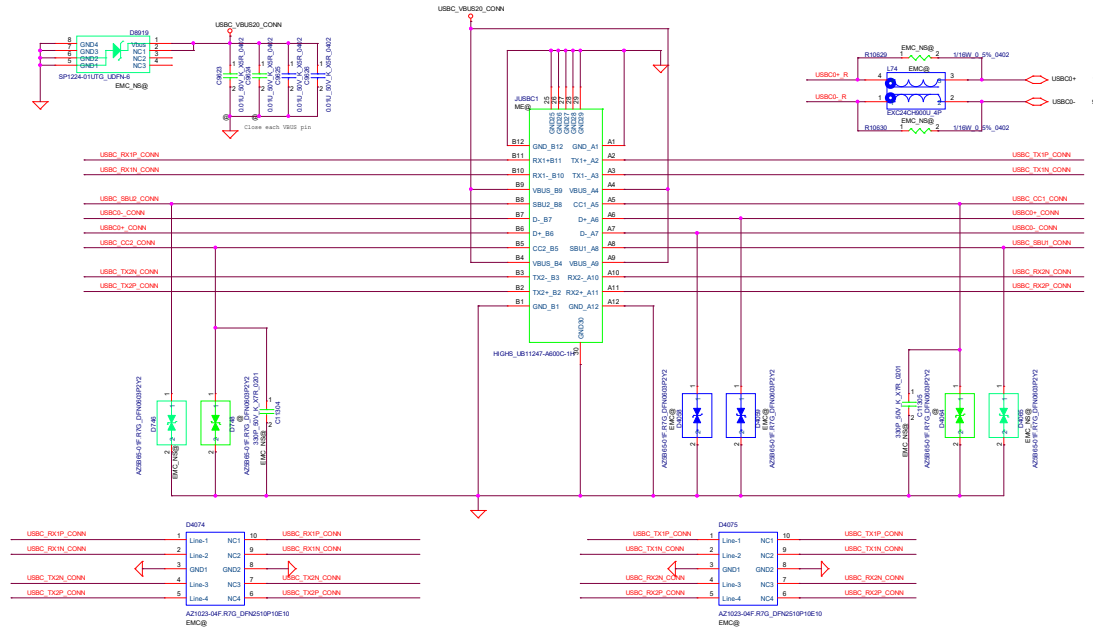


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| | | | | Customer | Drift AMD 3 | | | |
| | | | | Date | Tuesday, January 26, 2021 | | | Sheet 23 of 68 |




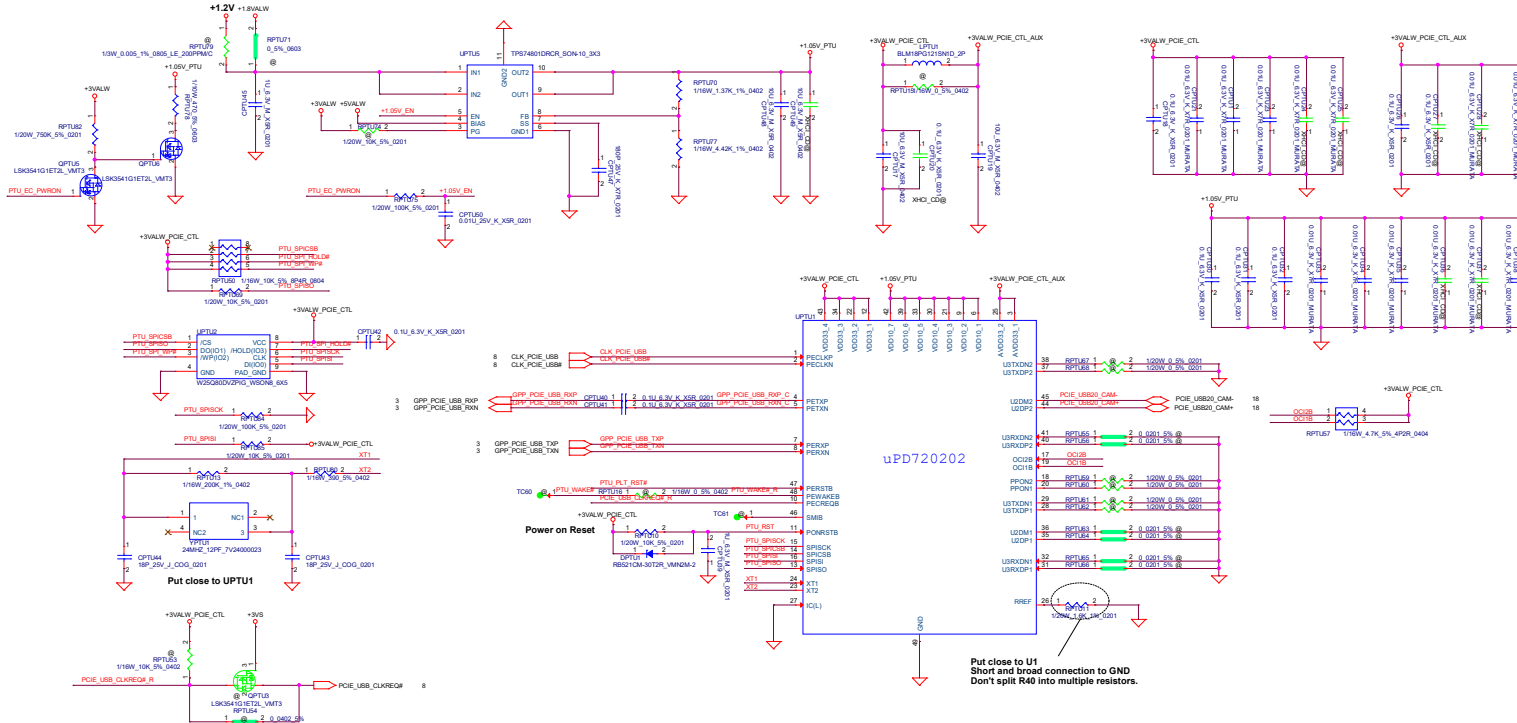
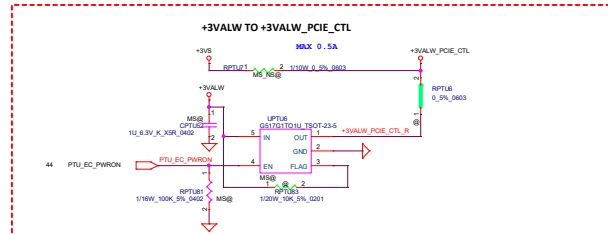
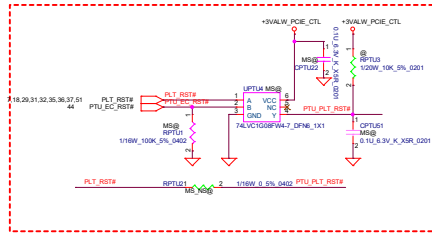


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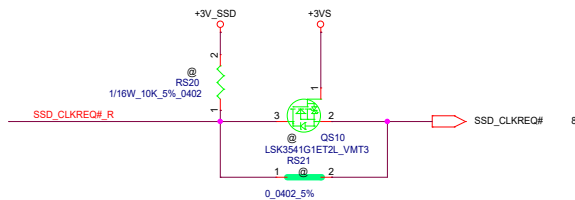
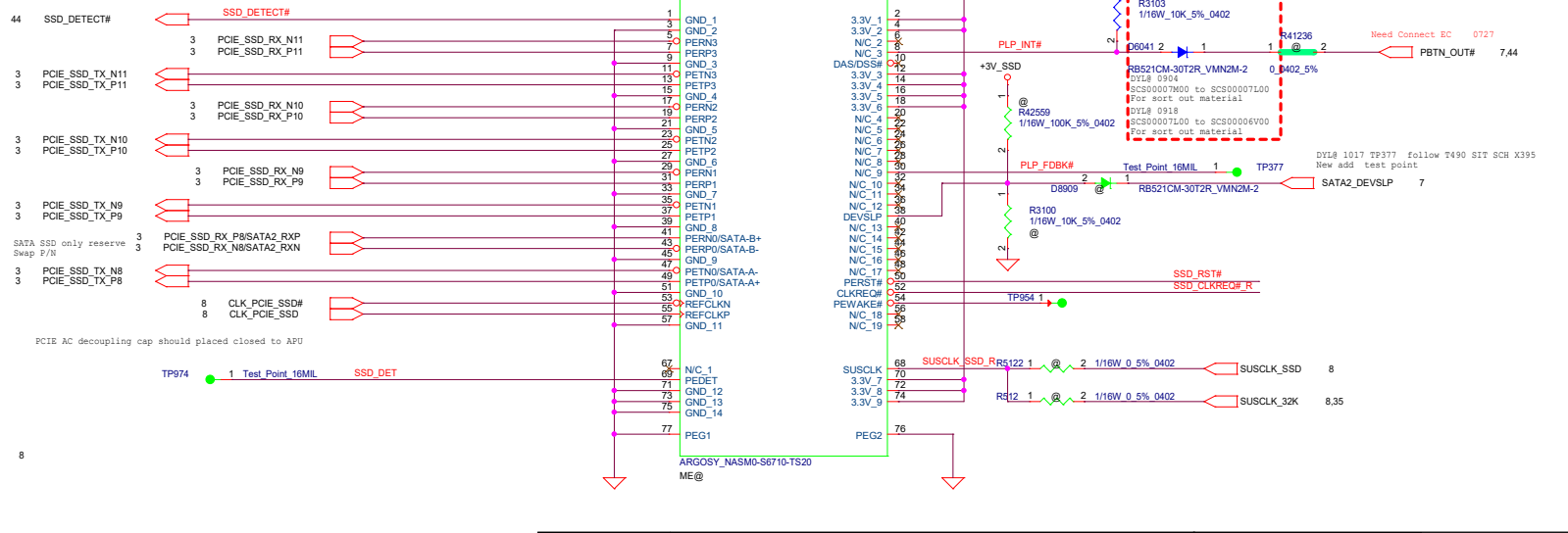
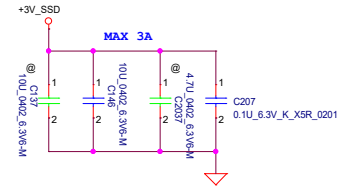
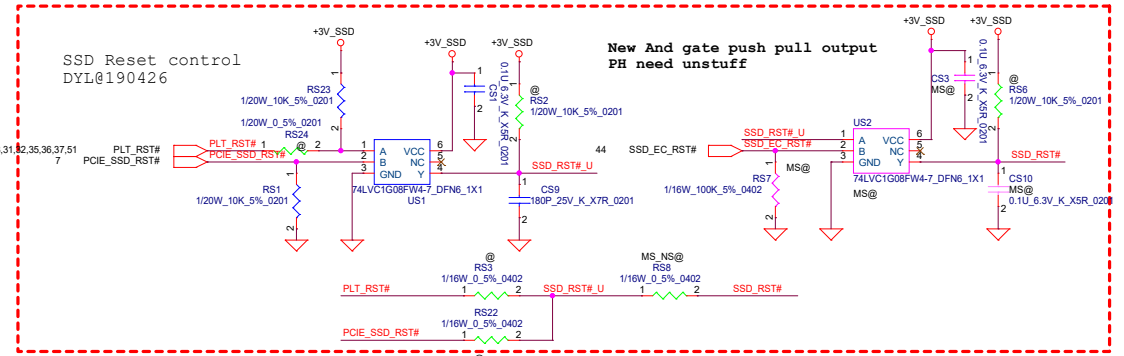
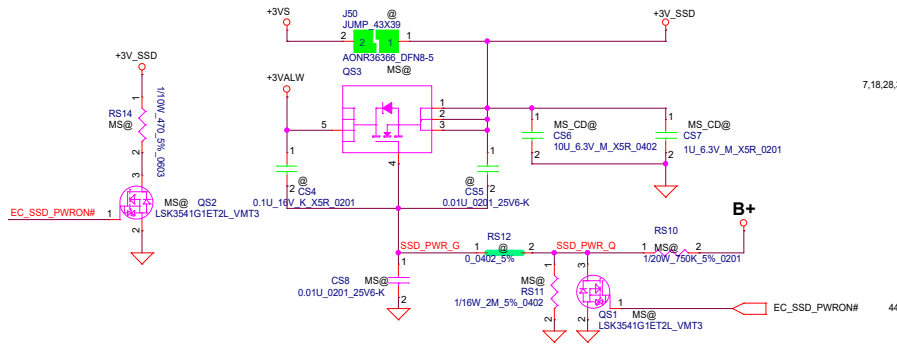
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|---|---|---|---|---|
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| D | | | | D |
| C | | | | C |
| B | | | | B |
| A | | | | A |
| 5 | 4 | 3 | 2 | 1 |
| | | | | 1 |


| | | | | | | |
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| | | | | B | Drift AMD 3 | 0.2 |
| | | | | Date: | Tuesday, January 26, 2021 | Sheet 27 of 68 |

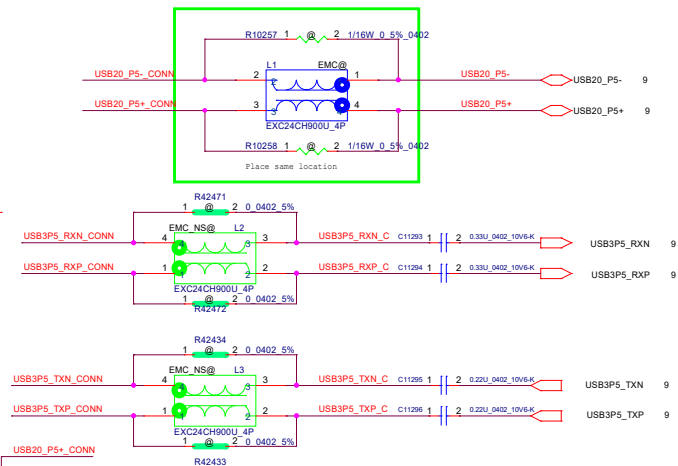
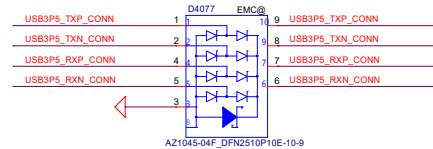
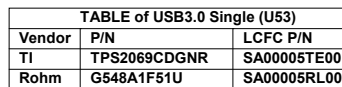



B+ 9V--13.6V

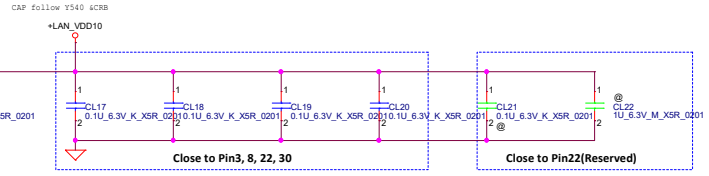
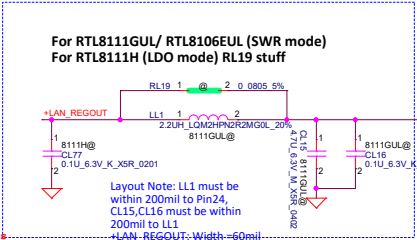
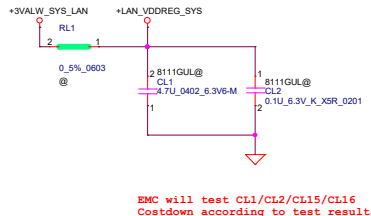
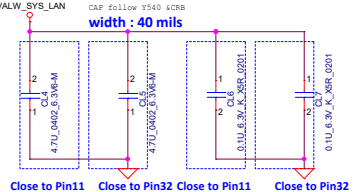
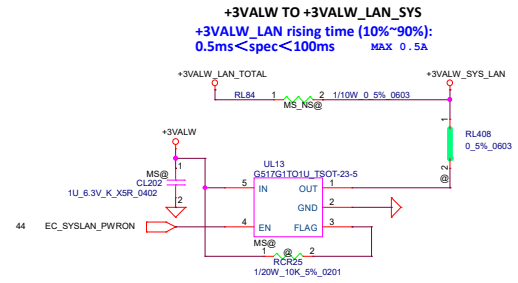
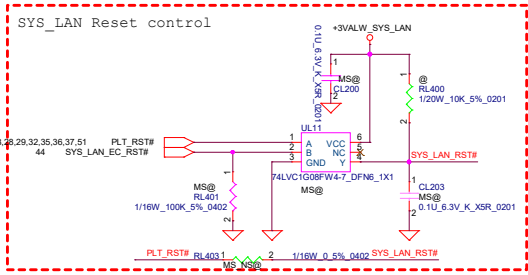
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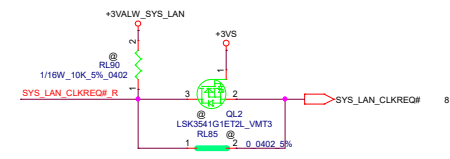
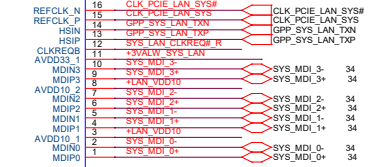
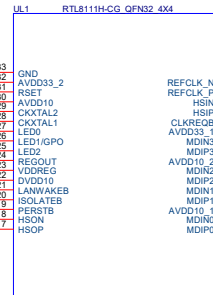
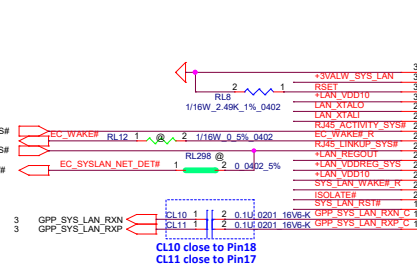
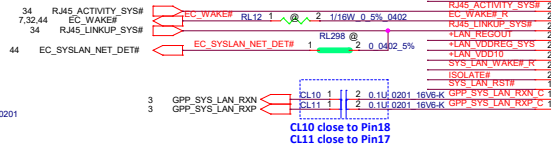
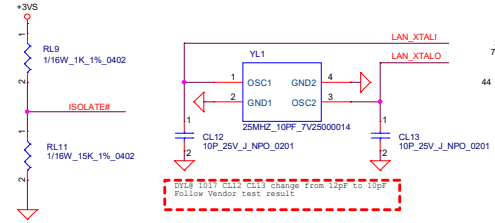
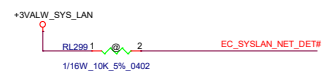
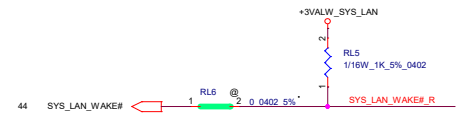
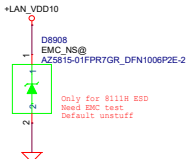
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| Date: | Tuesday, January 26, 2021 | Sheet | 29 | of | 68 | |

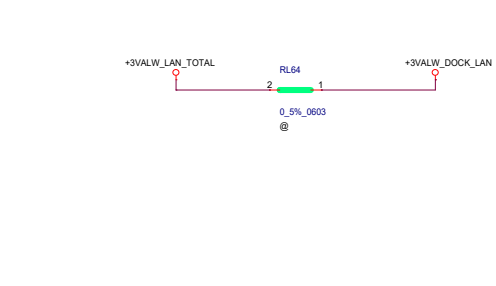
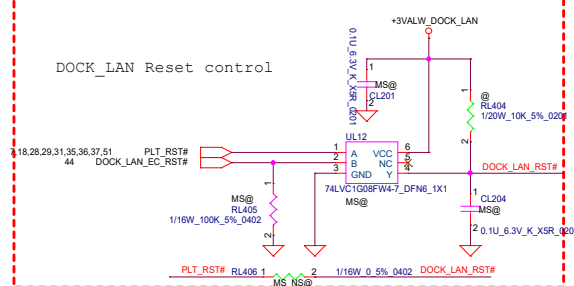
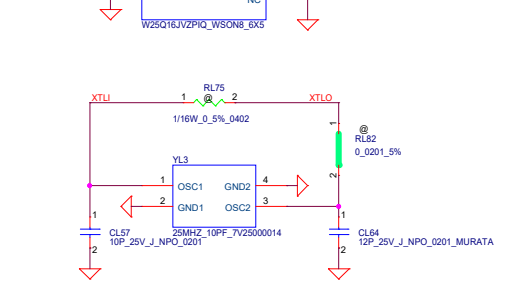
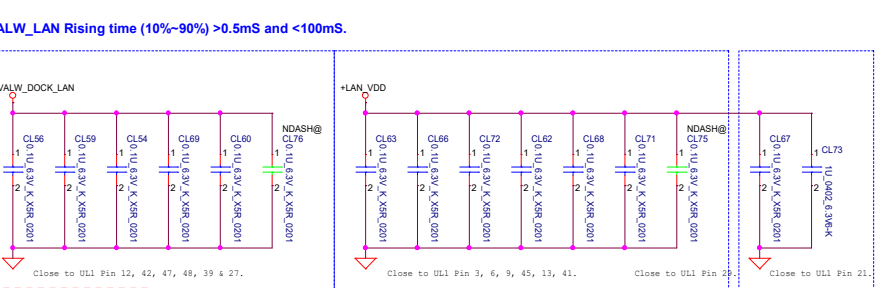
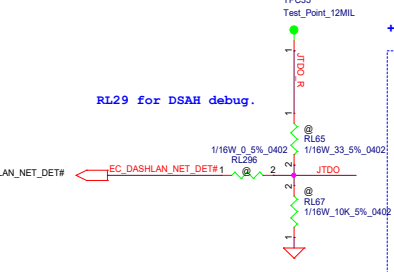
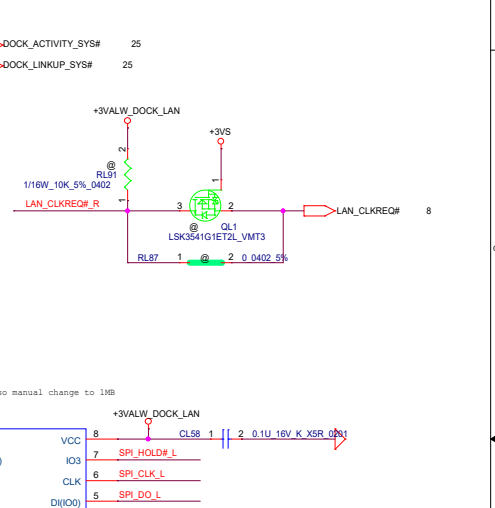
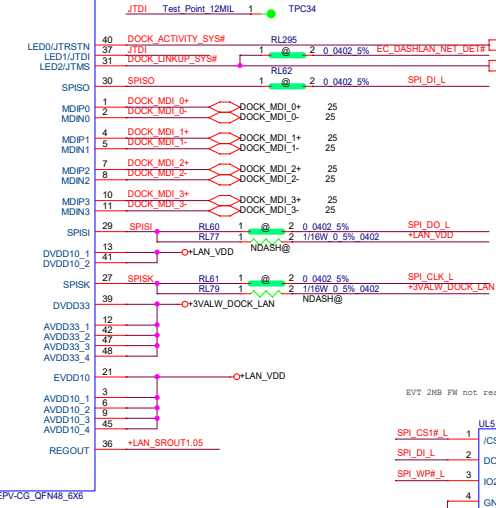
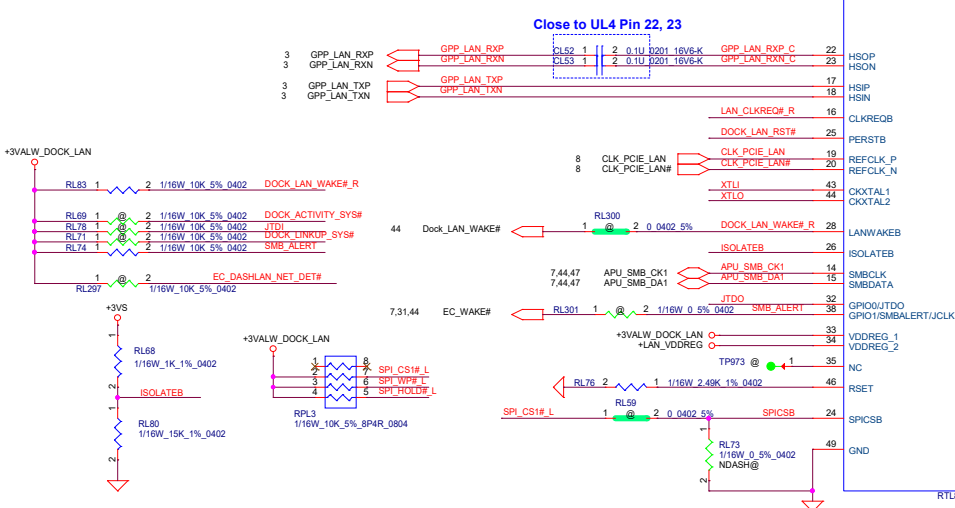
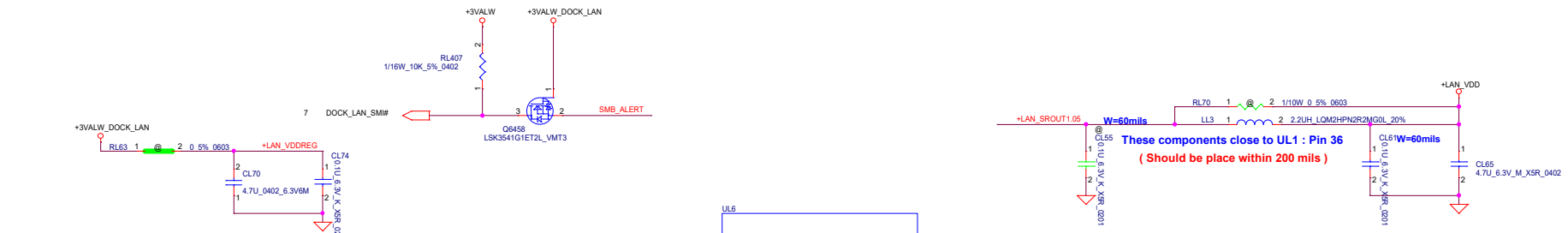


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D

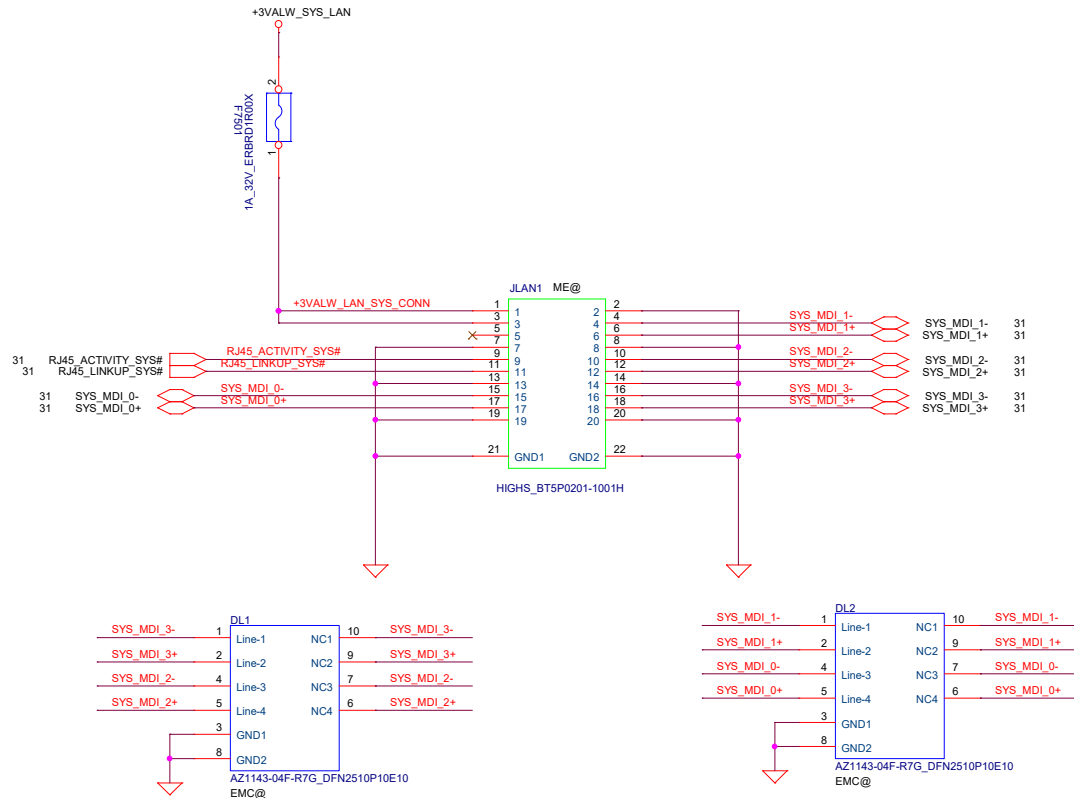
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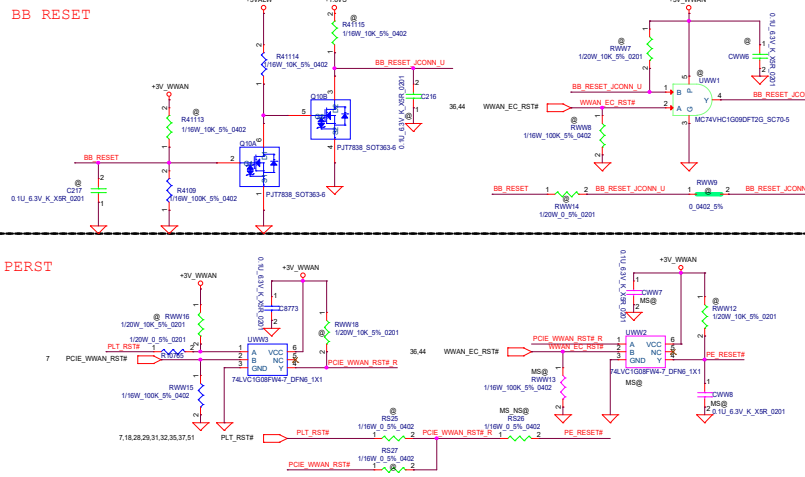
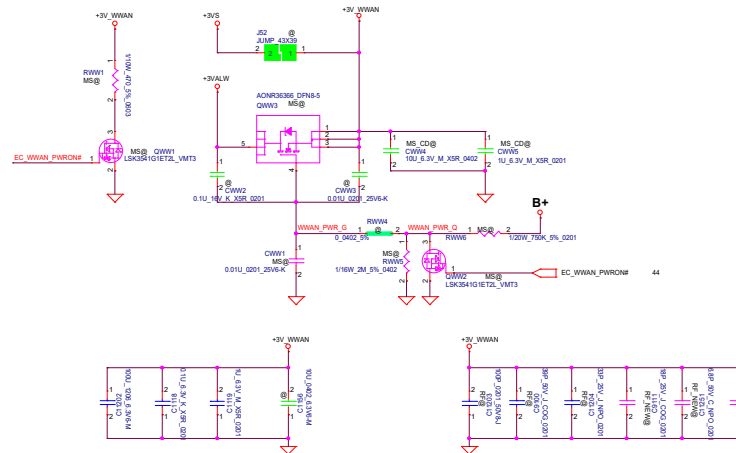
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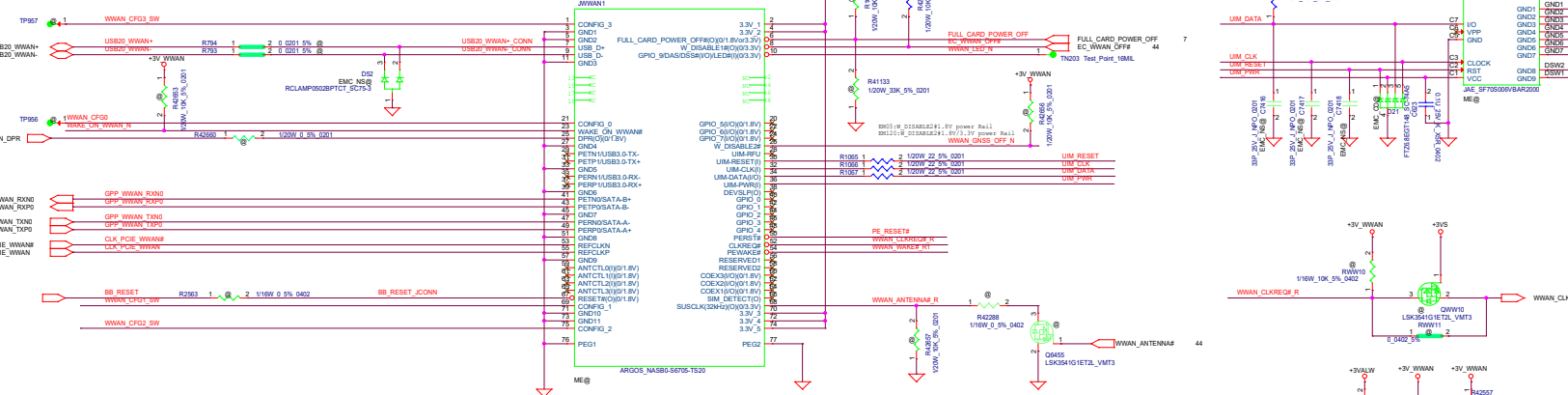
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| Date: Tuesday, January 26, 2021 | | | | | | |
| Sheet 33 of 68 | | | | | | |





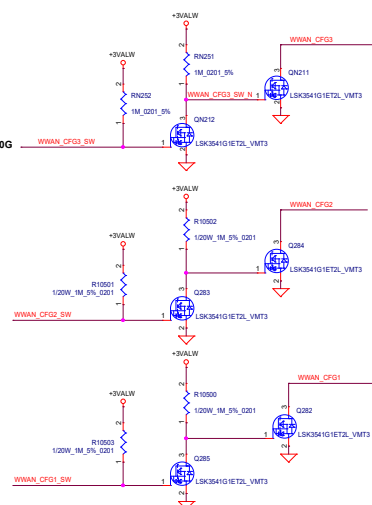


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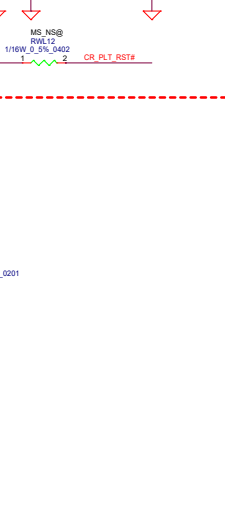
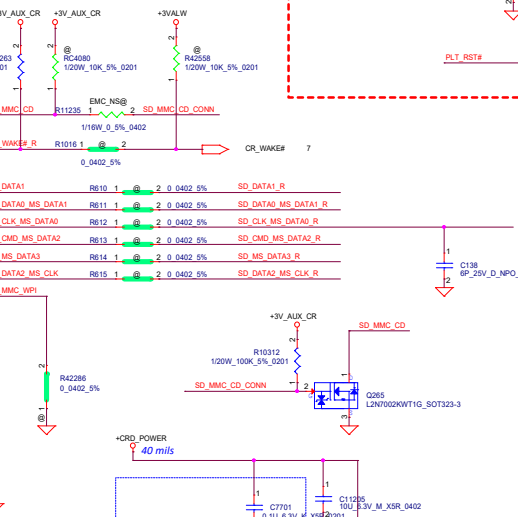
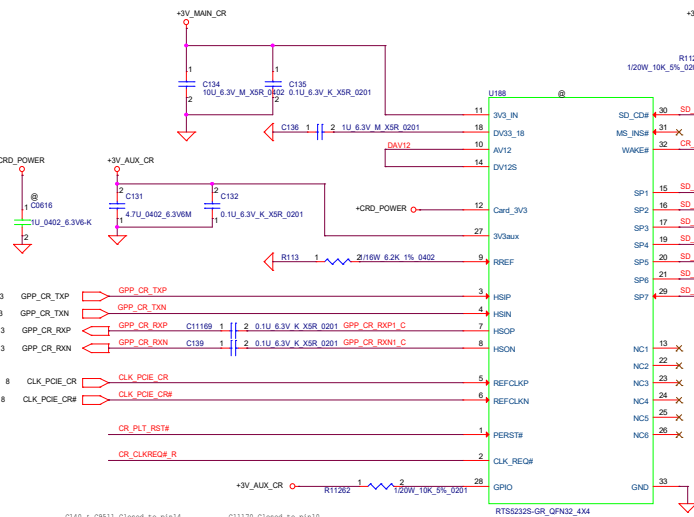
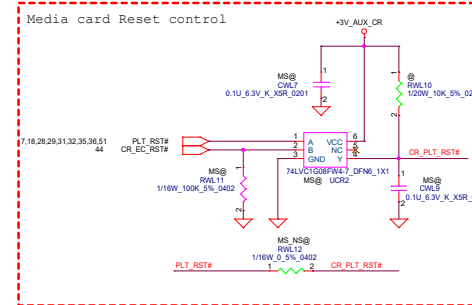
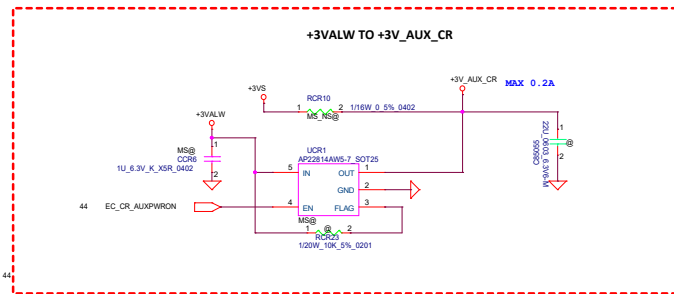
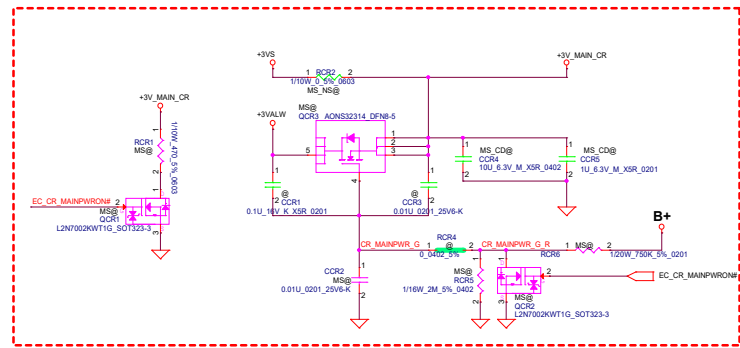


| TABLE: | | | | | | |
|---------|------------------------------|-------------------|-------------------|------------------|-------------------------------------|--------------------|
| State # | Module Configuration Decodes | | | | Module Type and Main Host Interface | Port Configuration |
| | CONFIG_0 (Pin 21) | CONFIG_1 (Pin 69) | CONFIG_2 (Pin 75) | CONFIG_3 (Pin 1) | | |
| 0 | GND | GND | GND | GND | SSD - SATA | N/A |
| 1 | GND | NC | GND | GND | SSD - PCIe | N/A |
| 2 | GND | GND | NC | GND | WWAN - PCIe | 0 |
| 3 | GND | NC | NC | GND | WWAN - PCIe | 1 |
| 4 | GND | GND | GND | NC | WWAN - USB 3.0 | 0 |
| 5 | GND | NC | GND | NC | WWAN - USB 3.0 | 1 |
| 6 | GND | GND | NC | NC | WWAN - USB 3.0 | 2 |
| 7 | GND | NC | NC | NC | WWAN - USB 3.0 | 3 |
| 8 | NC | GND | GND | GND | WWAN - SSIC | 0 |
| 9 | NC | NC | GND | GND | WWAN - SSIC | 1 |
| 10 | NC | GND | NC | GND | WWAN - SSIC | 2 |
| 11 | NC | NC | NC | GND | WWAN - SSIC | 3 |
| 12 | NC | GND | GND | NC | WWAN - PCIe | 2 |
| 13 | NC | NC | GND | NC | WWAN - PCIe | 3 |
| 14 | NC | GND | NC | NC | RFU | N/A |
| 15 | NC | NC | NC | NC | No Module Present | N/A |

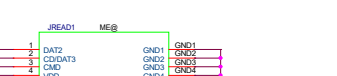
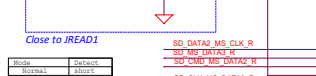
| | Module Configuration Decodes | | | |
|--------|------------------------------|------------------|-------------------|-------------------|
| | CONFIG_0 (Pin 21) | CONFIG_1 (Pin 1) | CONFIG_2 (Pin 75) | CONFIG_3 (Pin 69) |
| EM120G | GND | GND | NC | NC |
| EM05 | NC | GND | GND | GND |
| NA | NC | NC | NC | NC |
| SSD | GND | NC | GND | GND |



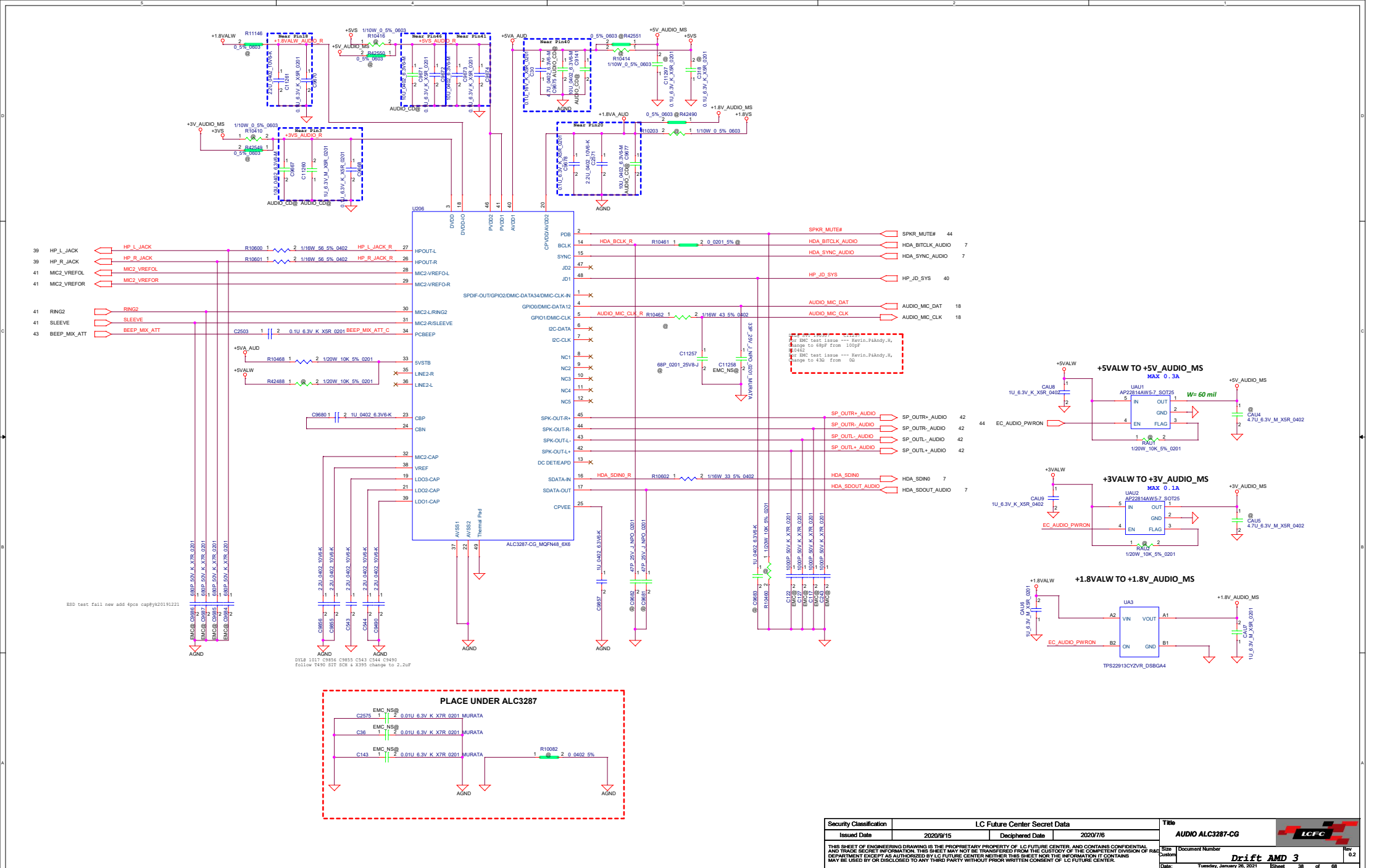
| | | |
|-----------------|---|-----------------|
| Vcc | 3.32V | |
| R10955 | 10K +/- 1% | |
| DEVICE_DETECT1# | 1.533V1.686V1.782V1.992V2.215V2.548V2.776V3.32V | |
| WWAN_CFG3 | V | V V V V X X X X |
| WWAN_CFG2 | V | V X X V V V X X |
| WWAN_CFG1 | V | X V X V X V X V |
| Configuration | EM05 | SSD EM120 NA |

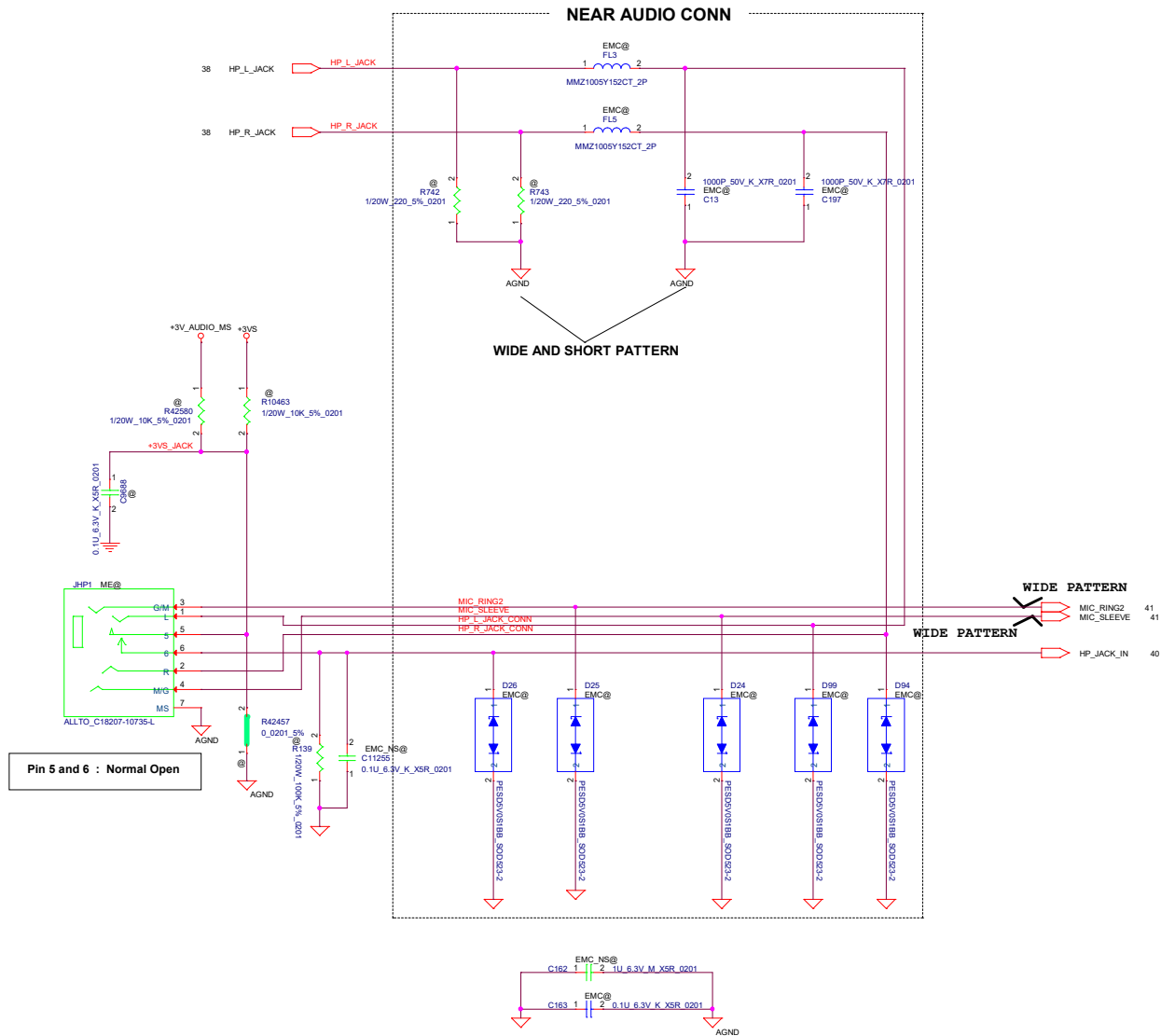


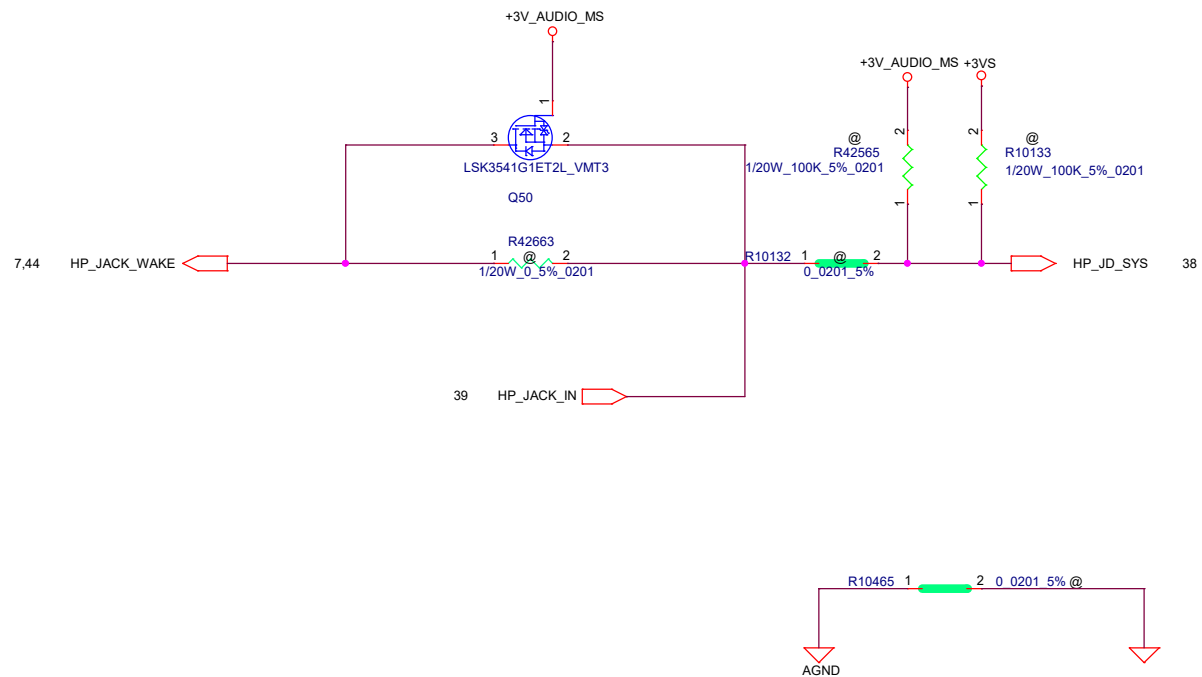
| Part Number | Vendor |
|-------------|----------------------|
| SA000077K00 | RTS5232S-GR REALTEK |
| SA00009JG10 | GL9750-OIYL4 GENESYS |




| | | | |
|----|---------|-----|--|
| 14 | DV12S | O | 1.2V power |
| 15 | SP1 | I/O | SD Data 1 (SD_D1) |
| 16 | SP2 | I/O | SD Data 0 (SD_D0) and MS Data 1 (MS_D1) |
| 17 | SP3 | I/O | SD Clock signal (SD_CLK) and MS Data 0 (MS_D0) |
| 18 | DV33_18 | O | 3.3V/1.8V power |
| 19 | SP4 | I/O | SD CMD signal (SD_CMD) and MS Data 2 (MS_D2) |
| 20 | SP5 | I/O | SD Data 3 (SD_D3) and MS Data 3 (MS_D3) |
| 21 | SP6 | I/O | SD Data 2 (SD_D2) and MS Clock signal (MS_CLK) |
| 22 | NC | | |
| 23 | NC | | |
| 24 | NC | | |
| 25 | NC | | |
| 26 | NC | | |

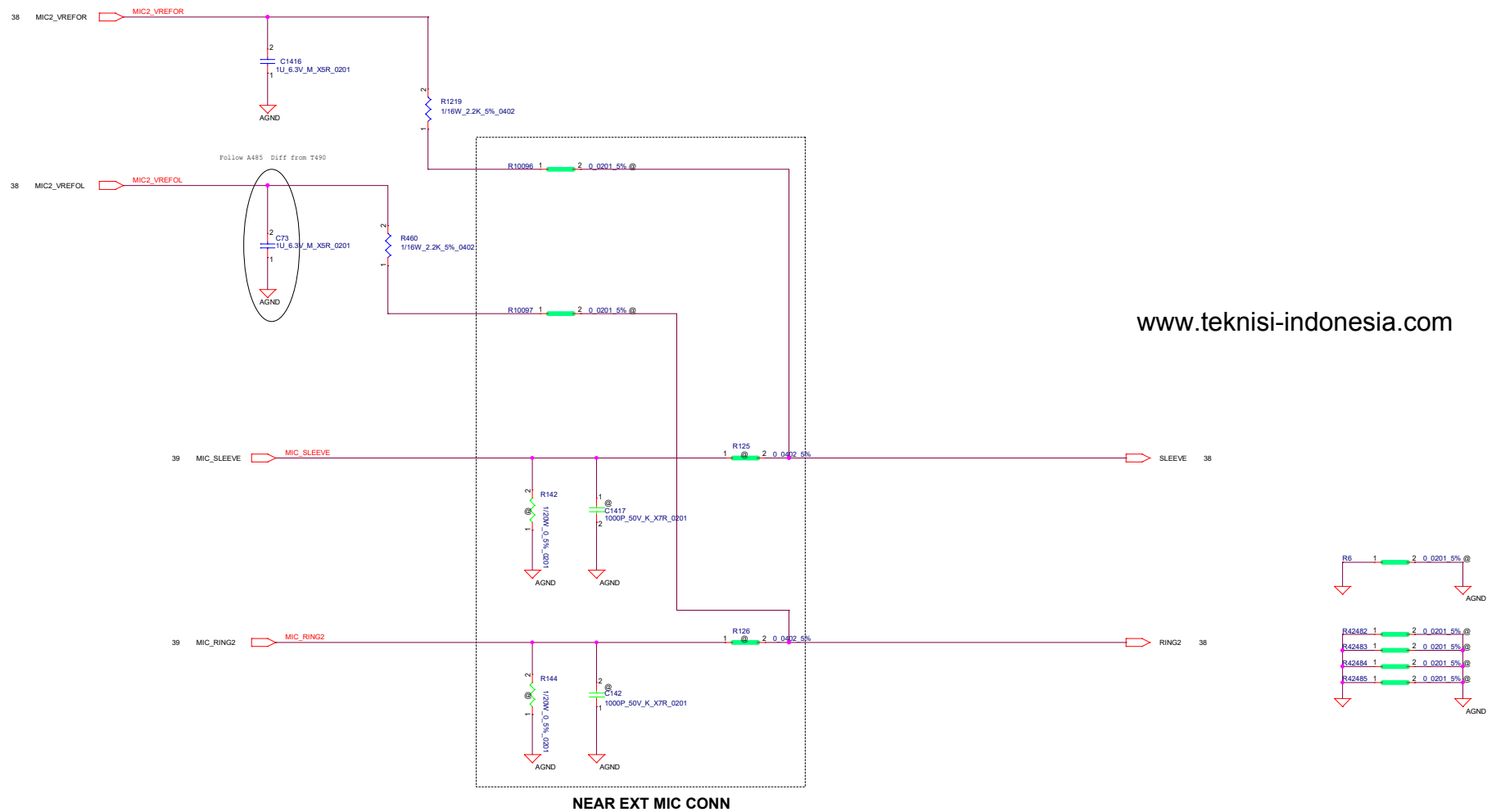


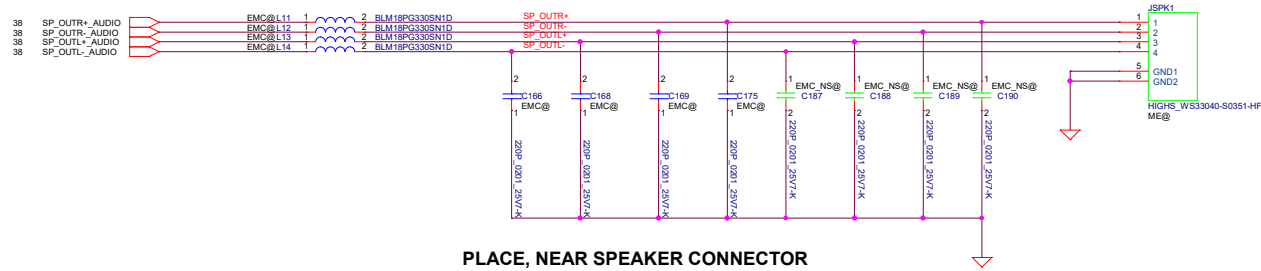





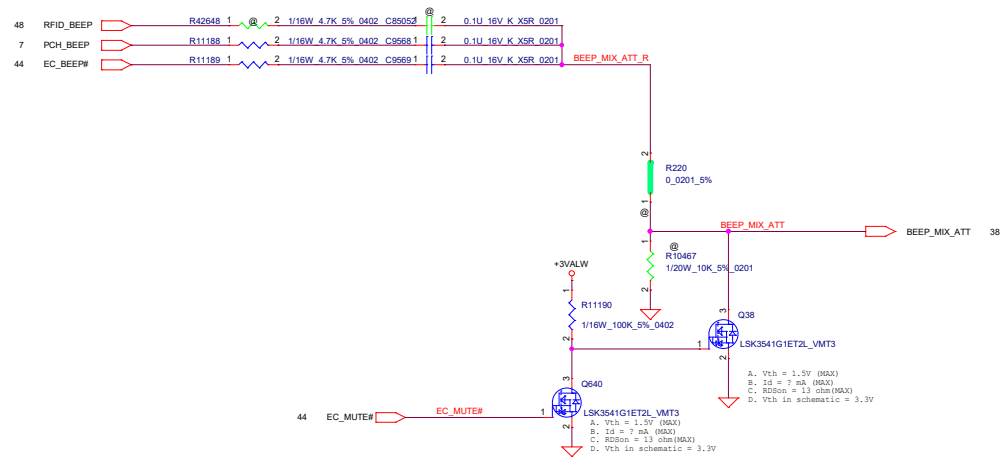
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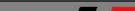
Drift AMD 3

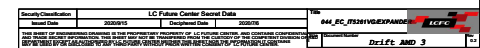


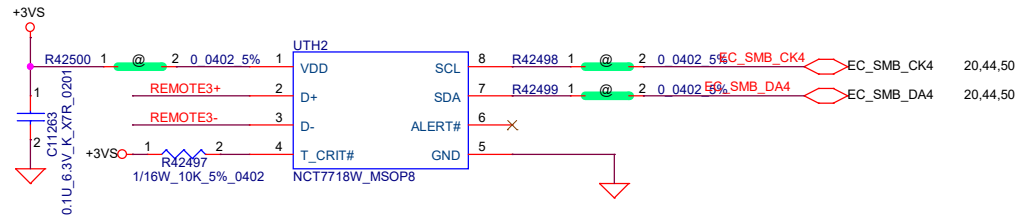


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| | | | | | C | | |
| Date: | | | | Tuesday, January 28, 2021 | Sheet | 42 | of 68 |



| | | | | | | | |
|--|-----------|------------------------------|----------|---------------------------|--|---|--|
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| Issued Date | 2020/8/15 | Deciphered Date | 2020/7/6 | AUDIO BEEP | | | |
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| Customer | | Document Number | | Drift AMD 3 | | Rev 0.2 | |
| | | Date | | Tuesday, January 28, 2021 | | 1 Sheet 43 of 68 | |

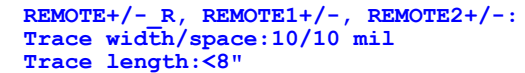




NCT7718W I2C/ SMBus™ address is 1001100xb (x is R/W bit).

| TABLE of UTH2 | | |
|---------------|----------|-------------|
| Vendor | P/N | LCFC P/N |
| Nuvoton | NCT7718W | SA000064D00 |
| FINTEK | F75397M | SA0000BT200 |

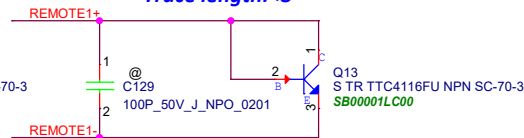
Close to UTH2




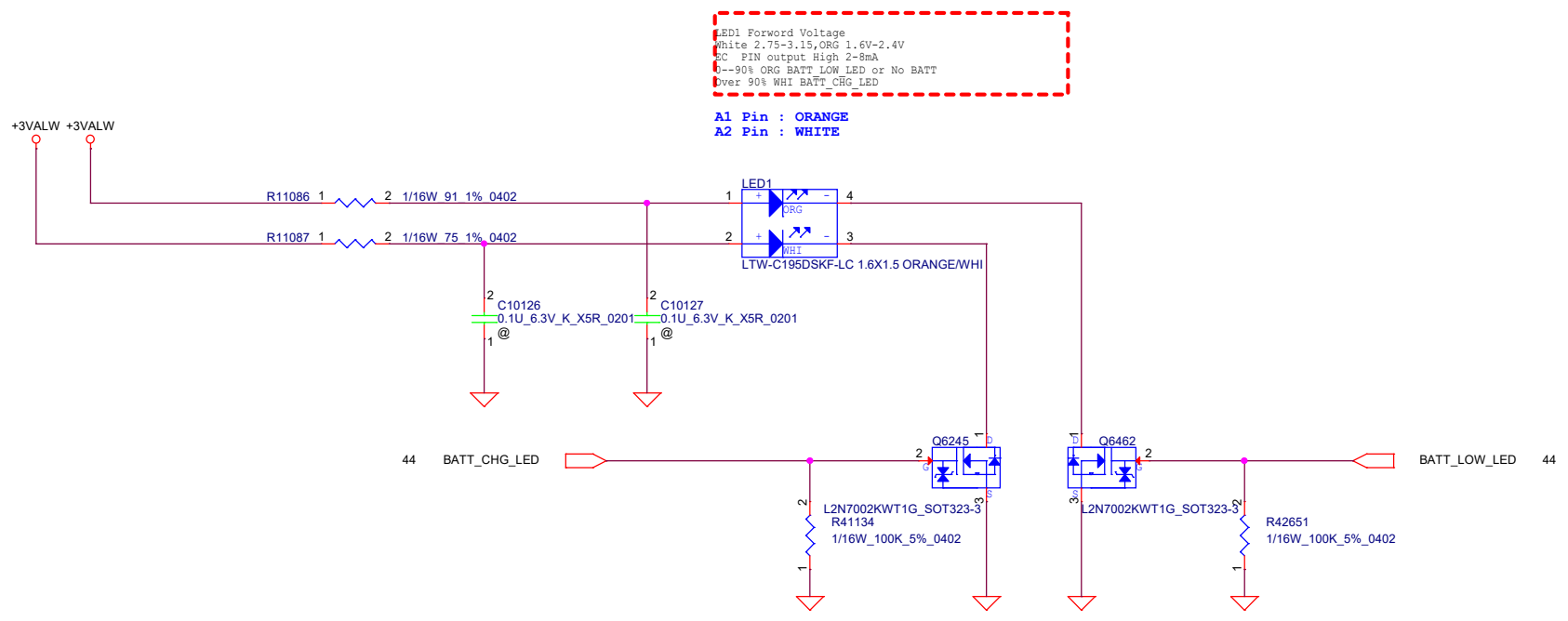
Close CHARGER



REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"




| | | | | | | |
|--|------------------------------|---------------------------|-------------|----------------|----|---|
| Security Classification | LC Future Center Secret Data | | | Title | |  |
| Issued Date | | Deciphered Date | | THERMAL SENSOR | | |
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| Size | Document Number | | Drift AMD 3 | | | Rev |
| 3 | | | | | | 0.2 |
| Date: | | Tuesday, January 26, 2021 | | Sheet | 45 | of 68 |

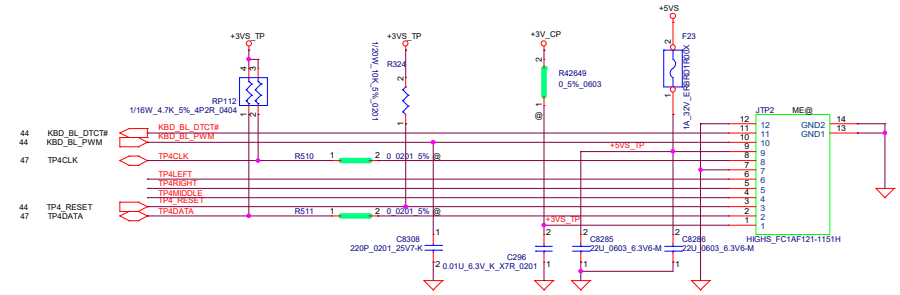
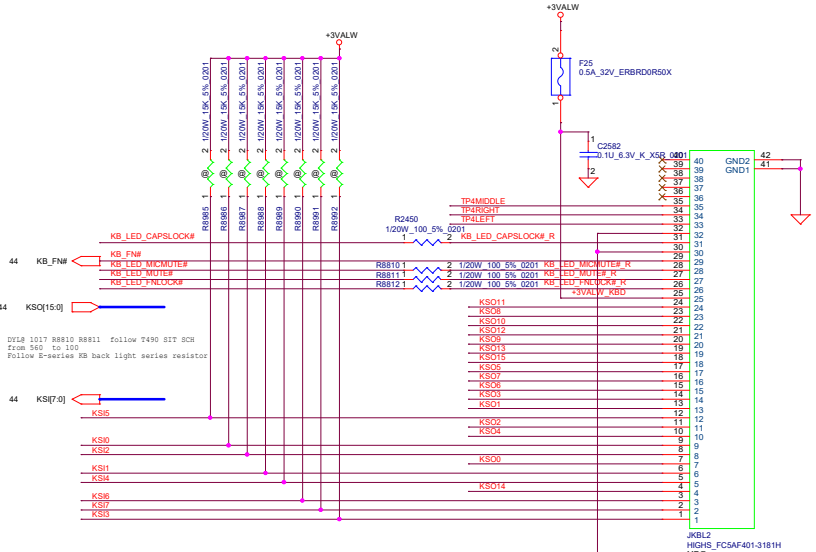
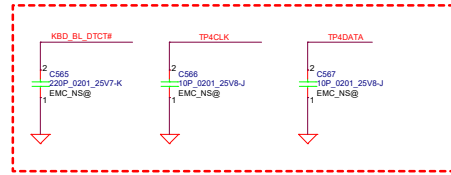
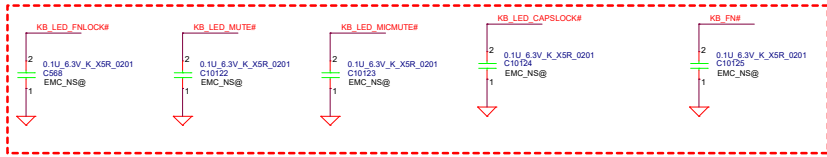


LED1 Forward Voltage
White 2.75-3.15, ORG 1.6V-2.4V
EC PIN output High 2-8mA
0--90% ORG BATT LOW LED or No BATT
Over 90% WHI BATT_CHG_LED

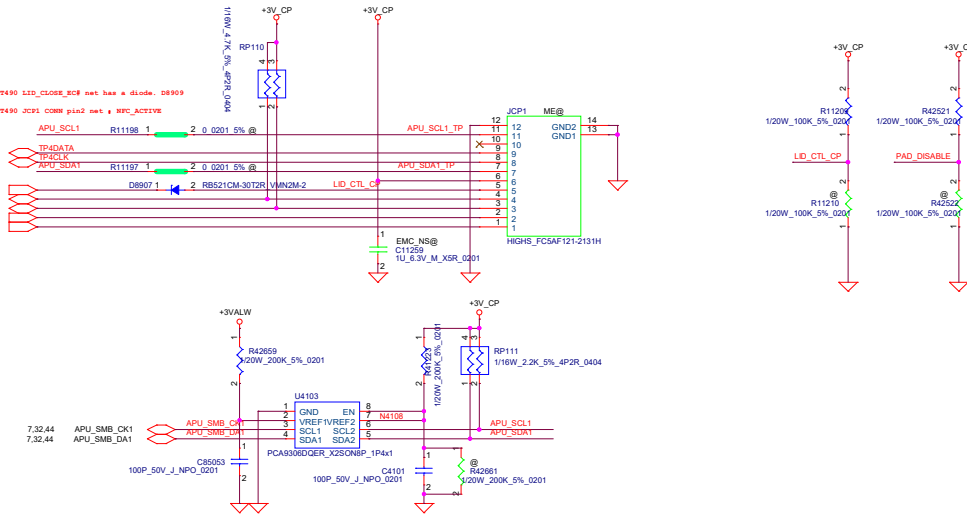
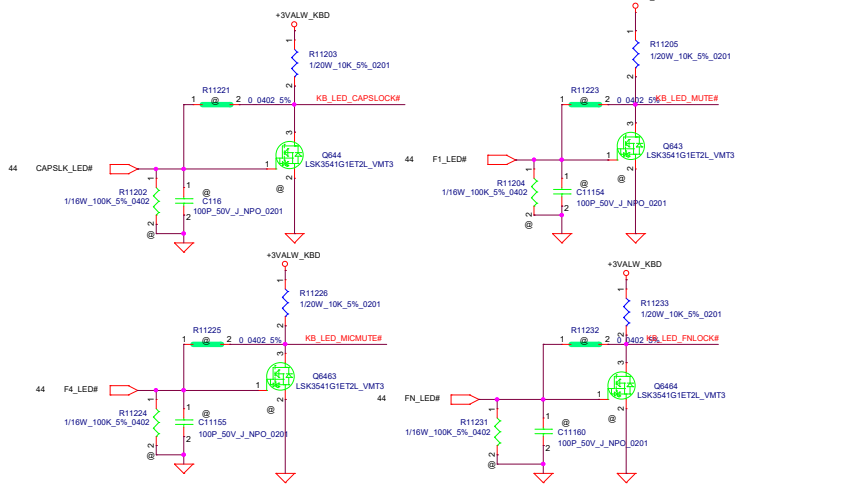
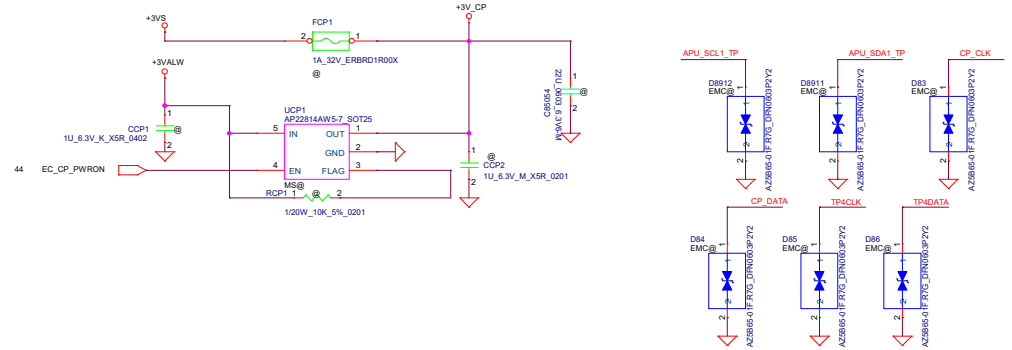
A1 Pin : ORANGE
A2 Pin : WHITE

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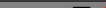
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|---|-----------------|------------------------------|-------------|------------|-----|-------|----|---|--|
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| Issued Date | | Deciphered Date | | CHARGE LED | | | | | |
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| B | | | | | | | | | |
| Date: | | Tuesday, January 26, 2021 | | Sheet | 46 | of | 68 | | |



Keyboard_Track Ponit





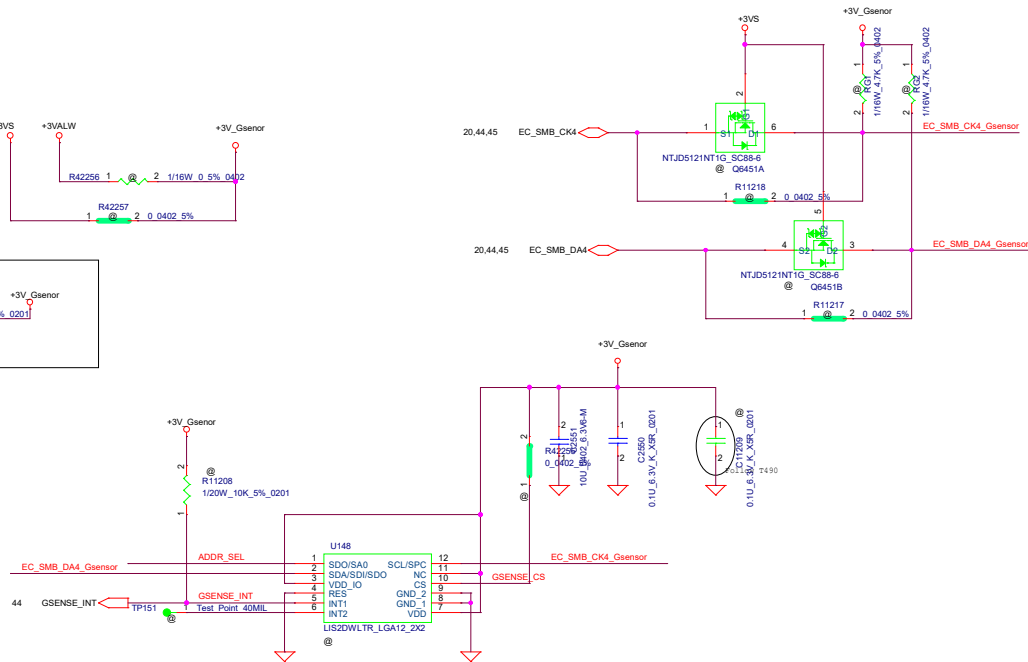
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|--|------------------------------|-----------------|----------|-----------------------------------|---------------------------------------|---|
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| Issued Date | 2020/9/15 | Deciphered Date | 2020/7/6 | FAN CONNECTOR | | |
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| | | | | Doc C | Document Number Drift AMD 3 | |
| | | | | Date Tuesday, January 26, 2021 | Sheet 49 of 68 | |

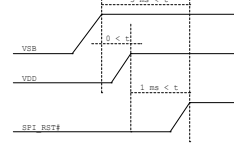


TABLE

| P/N | ADDR_SEL | Address |
|-----------|----------|--|
| LIS2DWLTR | H L | 32h (W) & 33h (R) 30h (W) & 31h (R) |
| BMA280 | H L | 3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R) |

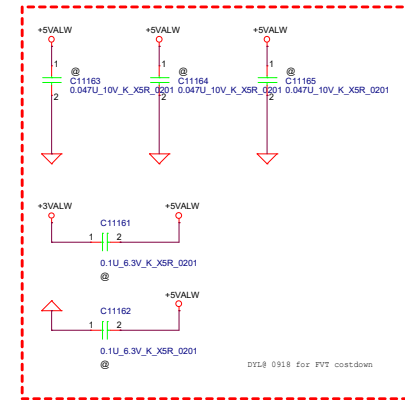
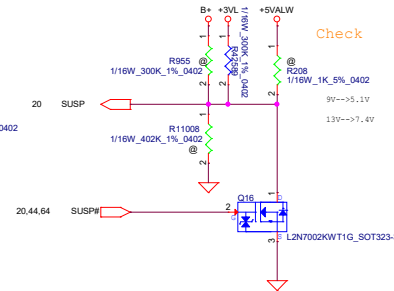
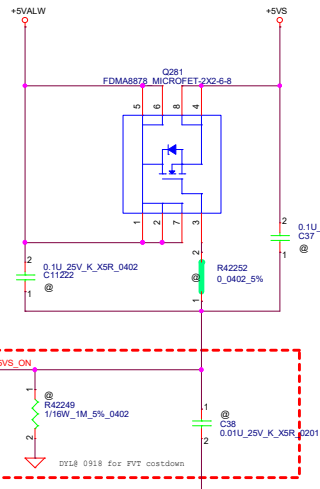
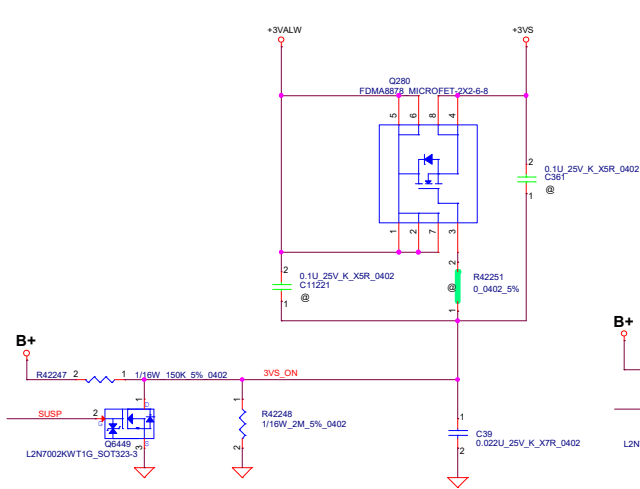
| TABLE of G-Sensor (U148) | | |
|--------------------------|-----------|-------------|
| Vendor | P/N | LCFC P/N |
| ST | LIS2DWLTR | SA00009AQ00 |
| BOSH | BMA280 | SA0000A1600 |





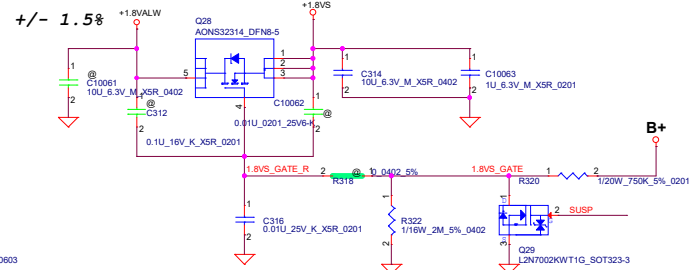
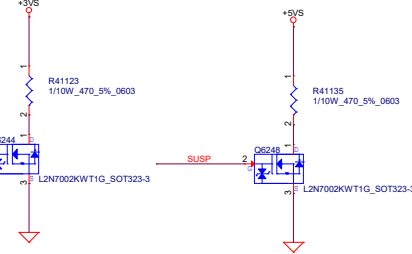
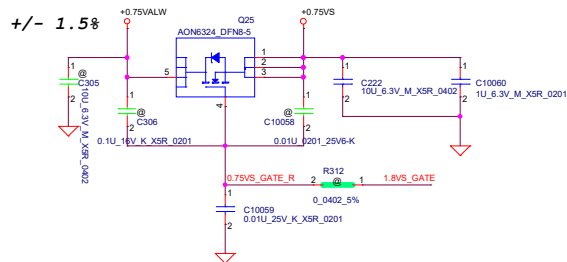
| Pin No | TCG PTP Spec (v38) | Nuvoton NPCT750LADYX | ST Micro ST33HTPH2X32AHD |
|--------|-----------------------|-------------------------|-----------------------------|
| 1 | VDD | VSB | NC |
| 2 | GND | NC | GND |
| 3 | NC | NC | NC |
| 4 | GPIO | GPIO/PP | NC |
| 5 | NC | NC | NC |
| 6 | GPIO | GPIO3 | GPIO |
| 7 | GPIO | NC | GPIO |
| 8 | VDD | VHIO | NC |
| 9 | NC | NC | NC |
| 10 | NC | NC | NC |
| 11 | NC | NC | NC |
| 12 | NC | NC | NC |
| 13 | GPIO | GPIO4 | NC |
| 14 | NC | NC | NC |
| 15 | NC | NC | NC |
| 16 | GND | GND | NC |
| 17 | SPI_RST# | RST# | SPI_RST# |
| 18 | SPI_PIRQ# | PIRQ#/GPIO2 | SPI_PIRQ# |
| 19 | SPI_CLK | SCLK | SPI_CLK |
| 20 | SPI_CS# | SCS#/GPIO5 | SPI_CS# |
| 21 | MOSI | MOSI#/GPIO7 | MOSI |
| 22 | VDD | VHIO | VPS |
| 23 | GND | GND | NC |
| 24 | MISO | MISO | MISO |
| 25 | NC | NC | NC |
| 26 | NC | NC | NC |
| 27 | NC | NC | NC |
| 28 | NC | NC | NC |
| 29 | SDA/GPIO1 | SDA/GPIO1 | NC |
| 30 | SDA/GPIO0 | SDA/GPIO0 | NC |
| 31 | NC | NC | NC |
| 32 | NC | NC | NC |

| TABLE of TPM | | |
|--------------|------------------|--------------|
| Vendor | P/N | LCFC P/N |
| Nuvoton | NPCT750LADYX | SA00008KS30 |
| ST | ST33HTPH2X32AHD4 | SA00000AB710 |

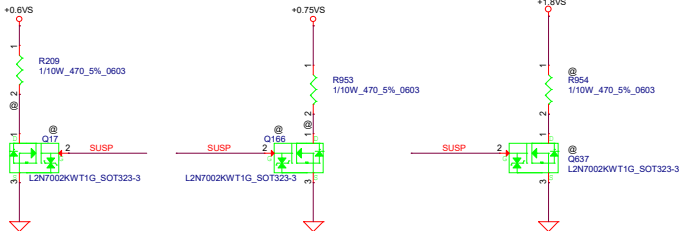


7/18 10/17 R42248 change from 1M to 2M
Follow 2395

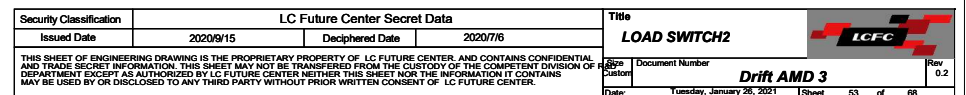
3V5V ON R42501 1 2 0 0402 5% 5V5V ON



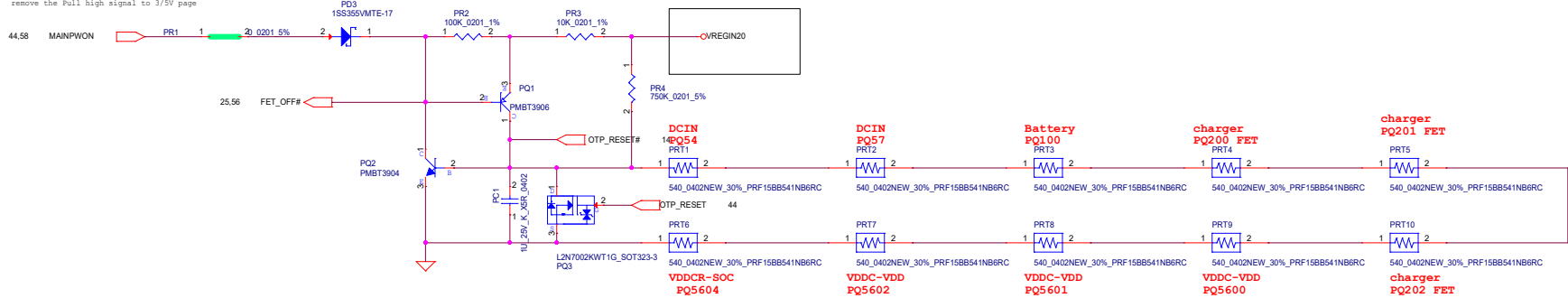
For DisCharge



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|--|--|--|--|------------------------------|--|--|--|----------------|--|
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| Date | | | | Tuesday, January 28, 2021 | | | | Sheet 52 of 68 | |

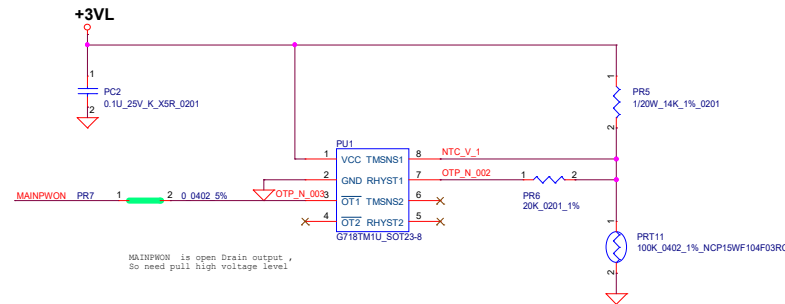


MAINPWON is open Drain output ,
So need pull high voltage level,
remove the Pull high signal to 3/5V page

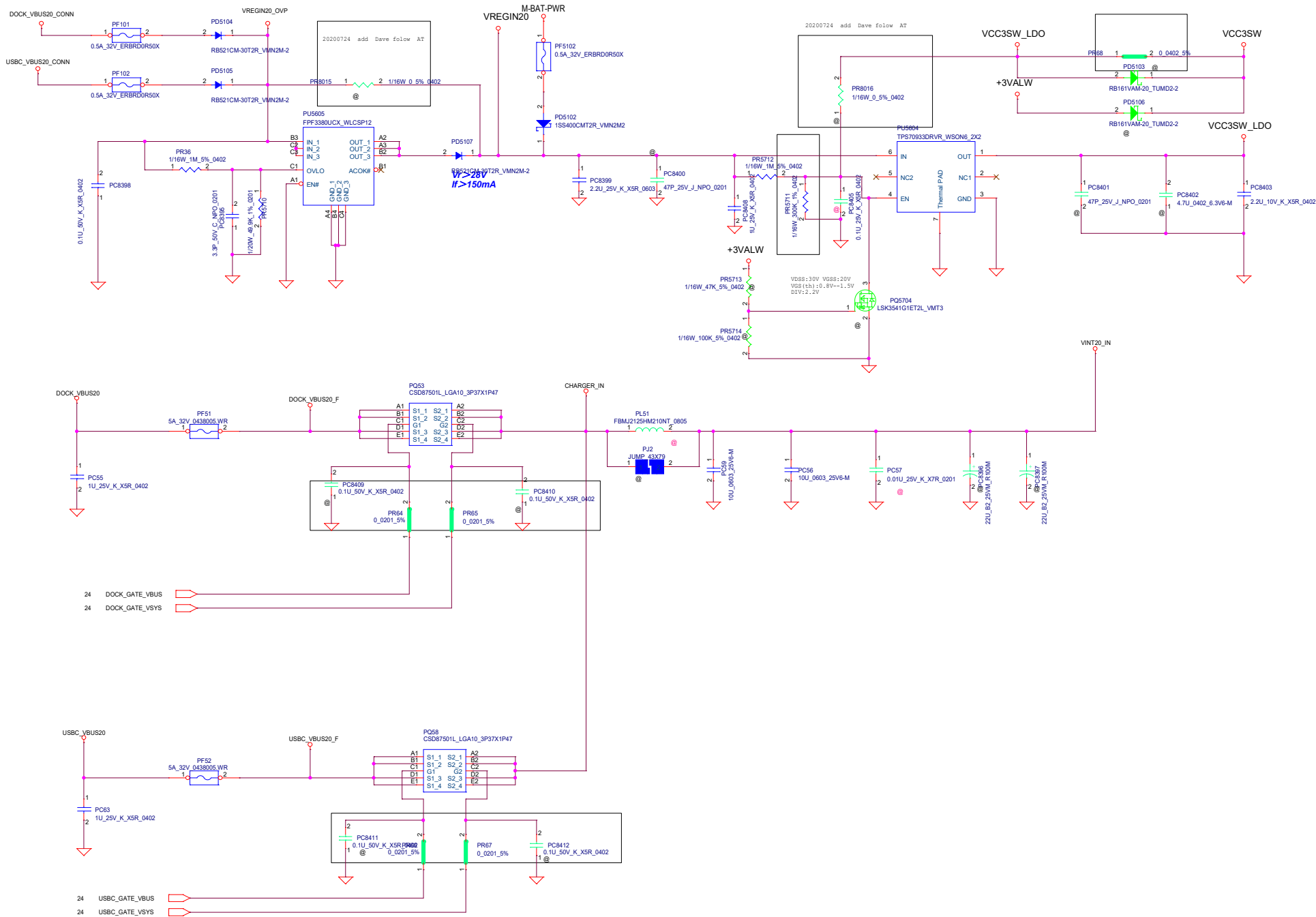


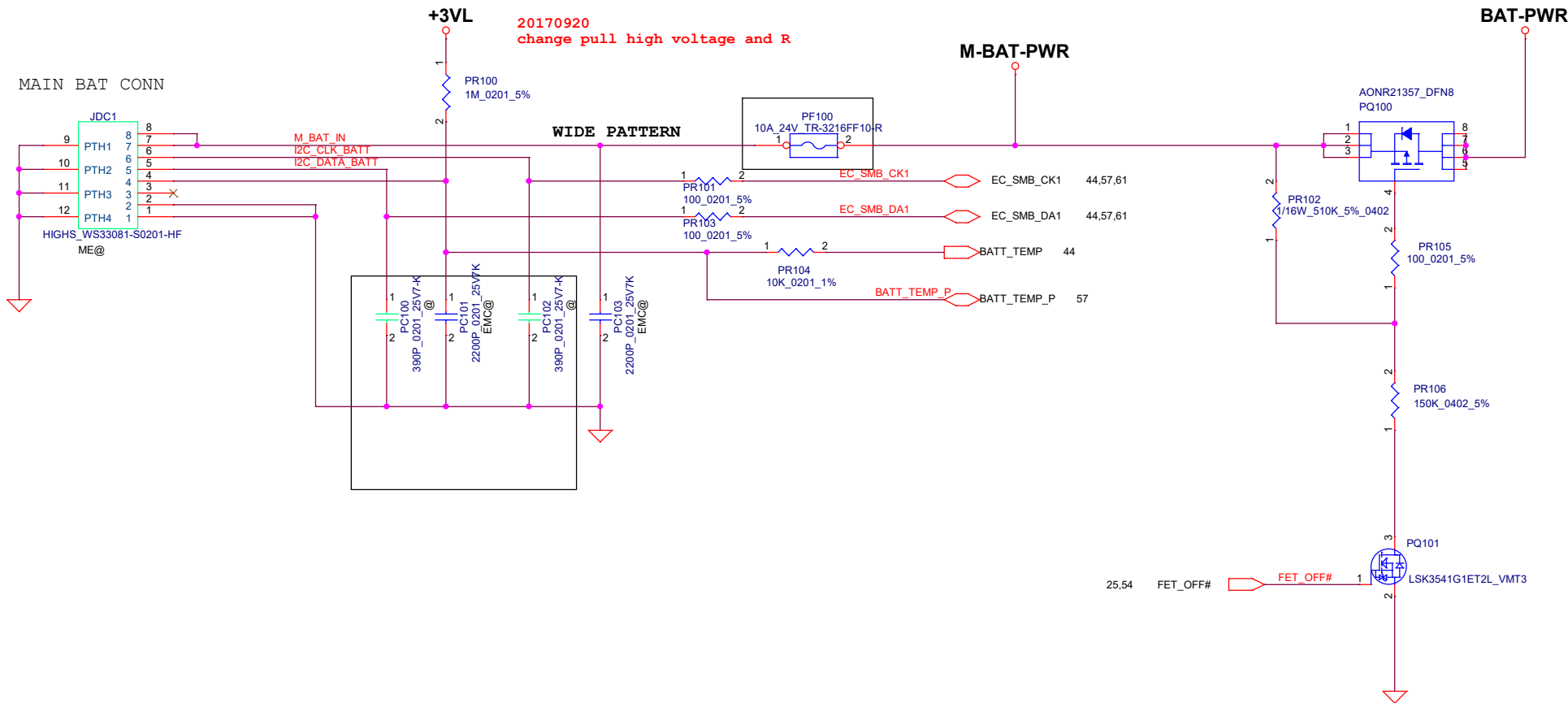
540_0402NEW_30%_PRF15BB541NB6RC
25~100Degree
0.54@25 Degree
1.2*0.54*k@85Degree
2*0.54 k@100 Degree
20*0.54 k@120Degree
100*0.54 k@130Degree
350*0.54 k@140Degree
Vbattery min =9V,Vbattery max =12.6V
Vthreshold min=0.65V,Vthreshold min=0.85V,
TotalR (PTC)*(VBatt-1.25)/(TotalR (PTC)+750)=0.65V
TotalR (PTC)max=59.8K~==110 times 0.54 k
TotalR (PTC)min=43.72K~==80times 0.54 k
Normal run 3Dmark
the max T maybe 85 Degree
the total R PTC= 1.2*0.54*10=12*0.54 k
if only one PTC over 130 degree,
the total PTC is 100*0.54K+11*0.54k,>80*0.54K
and over the min Vthreshold,and active the OTP
if only one PTC over 140 degree,
the total PTC is 350*0.54K>>80*0.54K
,can over the min Vthreshold
and active the OTP
so,the OTP function is ok

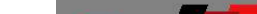
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PRT11 under CPU bottom side :
CPU thermal protection at 93 +/-3 degree C
Recovery at 56 +/-3 degree C





| | | | | | | |
|---|---------------------------|------------------------------|-------------|---------------|-----|---|
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| B | | | | | 0.2 | |
| Date: | Tuesday, January 26, 2021 | | Sheet | 56 | of | 68 |

VINT20_IN

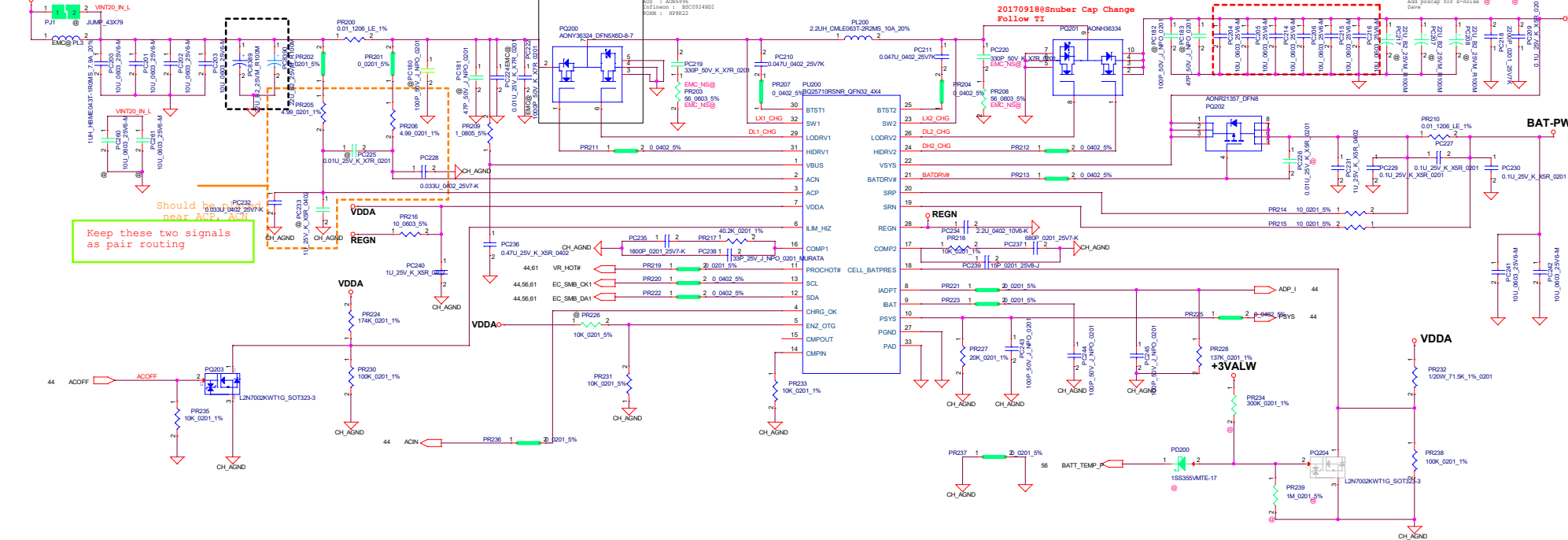


Table PL101

TOKO : FDSD0630-H-2R2M
Cyntec : CMLE063T-2R2MS

20170918Snubber Cap Change
Follow TI

MLCCs must be placed
symmetrically on Top and Bottom.

Add poscap for E-noise

Should be
near ACP, ACK

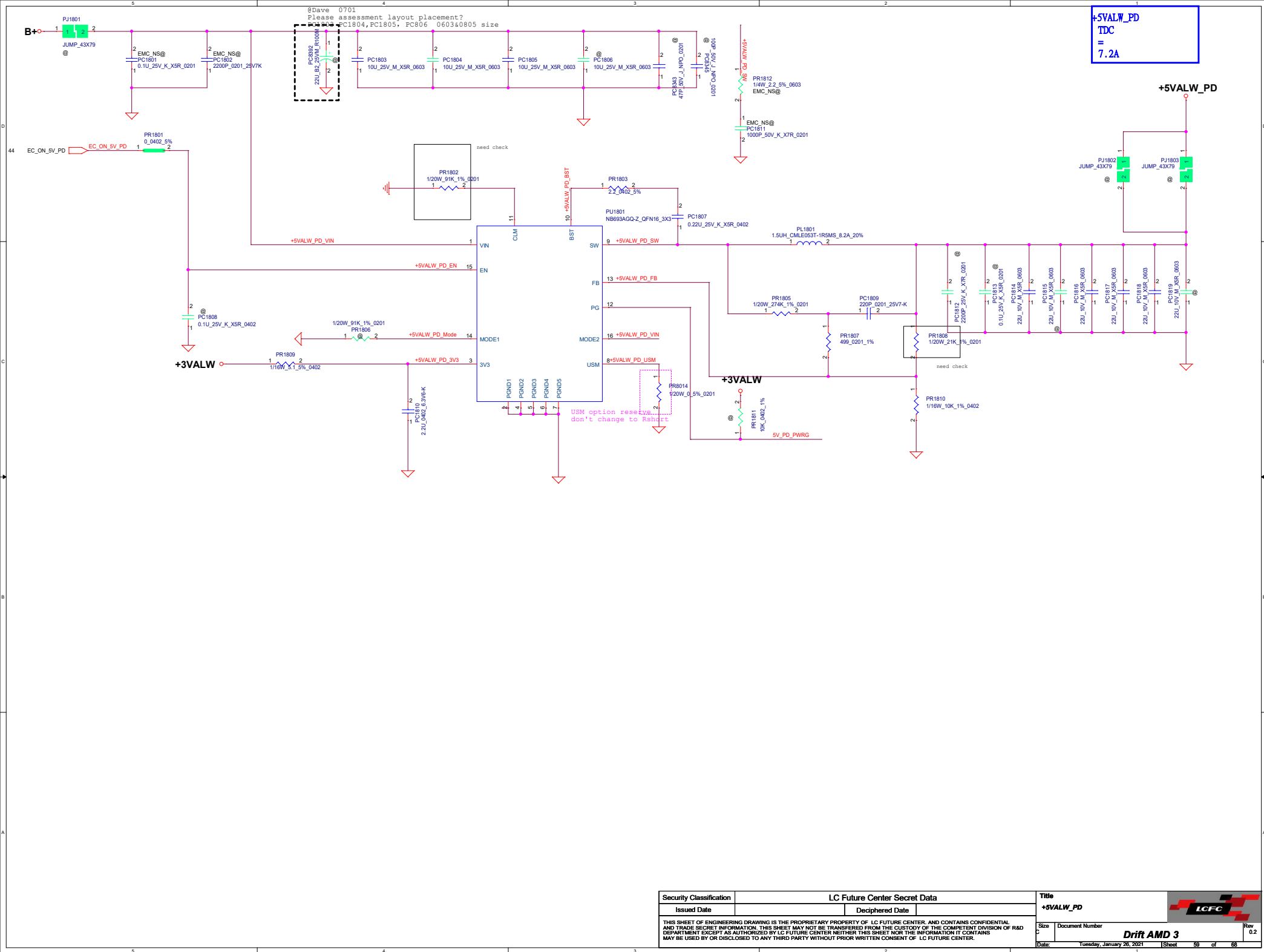
Keep these two signals
as pair routing

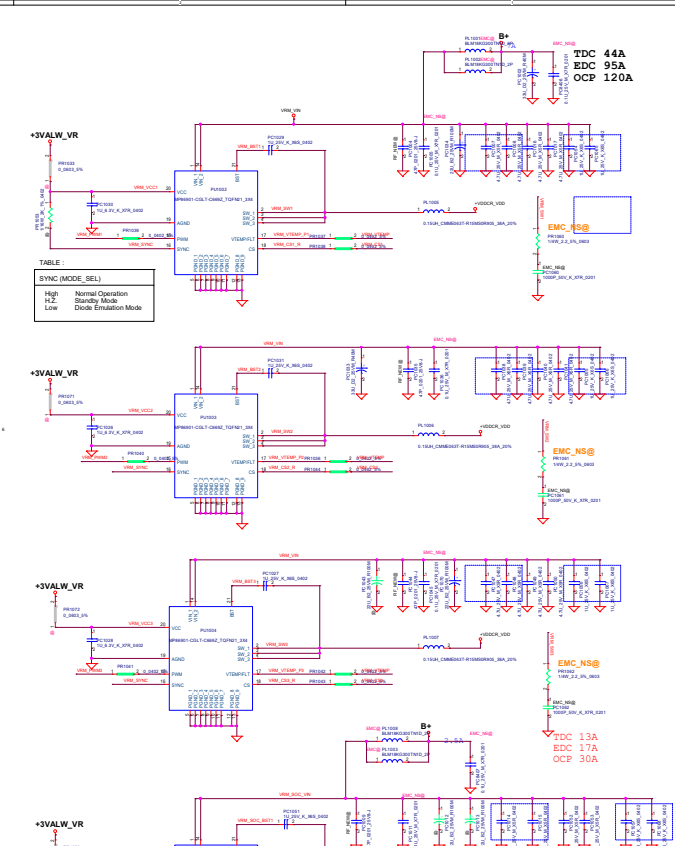
| # of CELL | VCELL_PRES | PR154 |
|-----------|------------|-------|
| 1-CELL | 1.5V | 301K |
| 2-CELL | 2.5V | 140K |
| 3-CELL | 3.5V | 71.5K |
| 4-CELL | 4.5V | 33.2K |

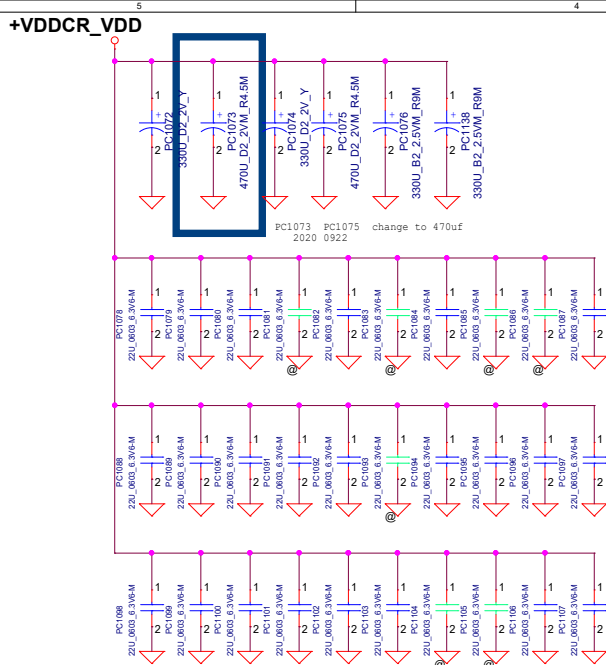
| IDPM | V (ILIM) | PR147 |
|-------|----------|-------|
| 500mA | 1.2V | 402K |
| 1.0A | 1.4V | 332K |
| 1.5A | 1.6V | 280K |
| 2.0A | 1.8V | 237K |
| 3.0A | 2.2V | 174K |
| 3.25A | 2.3V | 162K |

← LOGIC

| | | | |
|--|------------------------------|---------------------------|----------|
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| Issued Date | Deciphered Date | BATTERY CHARGER(BQ25700A) | |
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| Page | Document Number | Date | |
| 1 | Drift AMD 3 | Tuesday, January 26, 2021 | |
| | | Sheet | 97 of 98 |

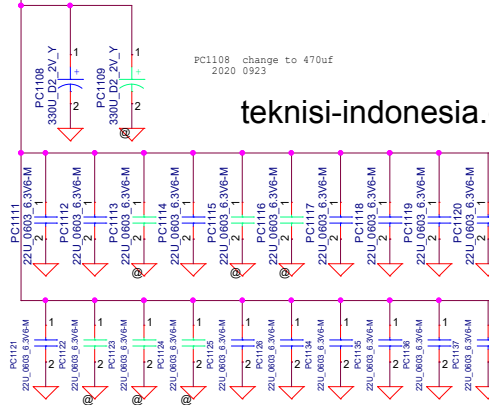







Note--Cezanne
330uF/9mohm*4pcs+330uF/6mohm*1
22uF/0603*23pcss

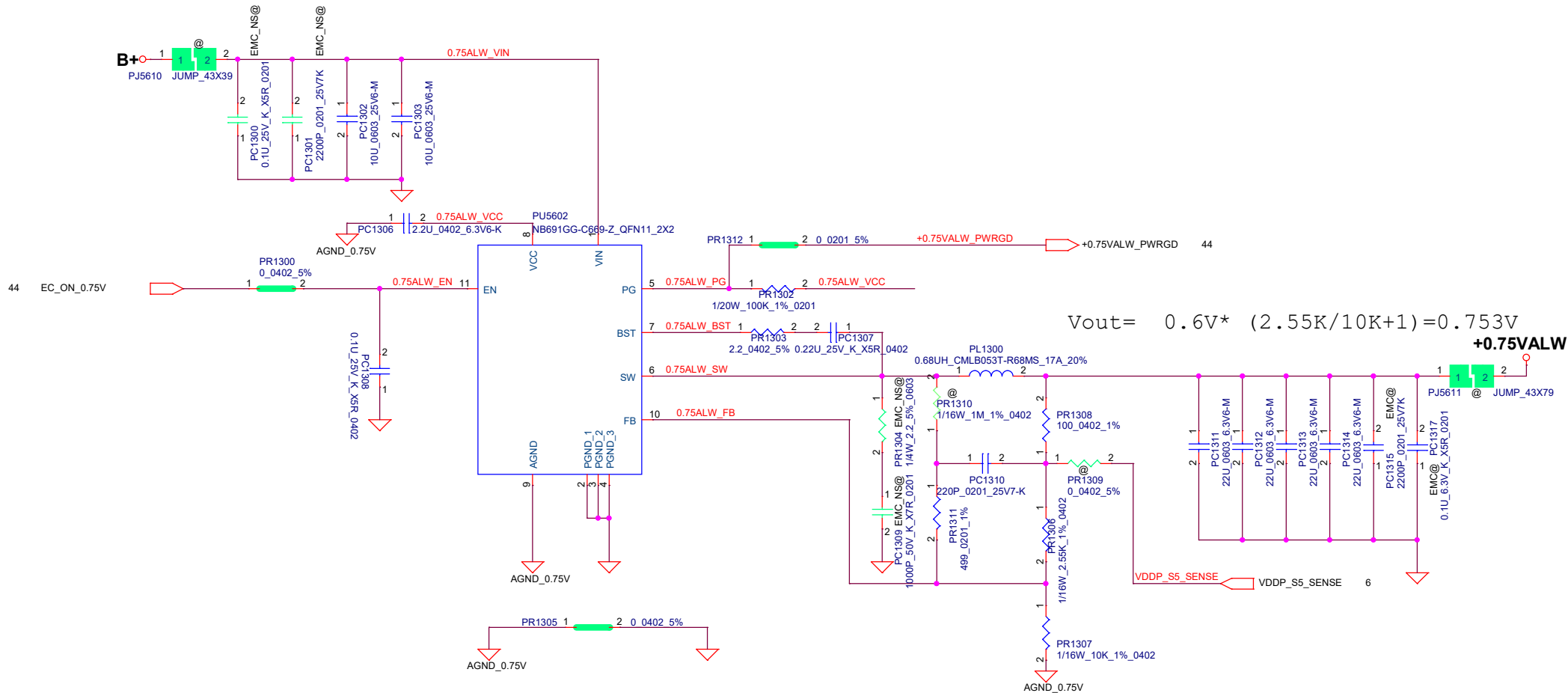
+VDDCR_SOC




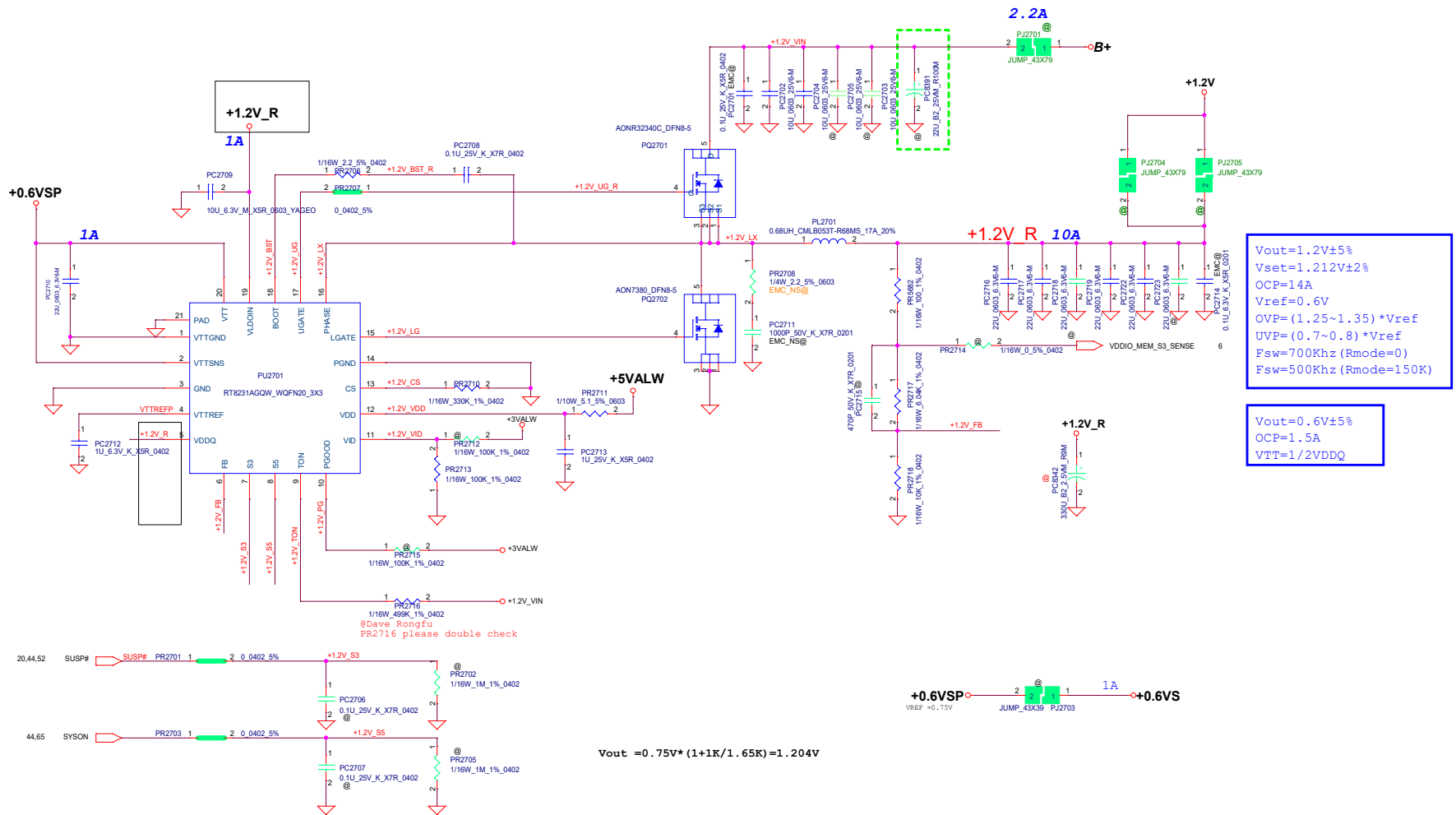
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Cezanne
330uF/9mohm*1pcs
22uF/0603*14 pcss

| | | | | | |
|--|-----------------|------------------------------|--|--|--|
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| Issued Date | | Deciphered Date | | VCORE_DECOUPLING_CAP  | |
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| Size | Document Number | | | Rev | |
| Custom | Drift AMD 3 | | | 0.2 | |
| Date: | | Tuesday, January 26, 2021 | | Sheet 62 of 68 | |

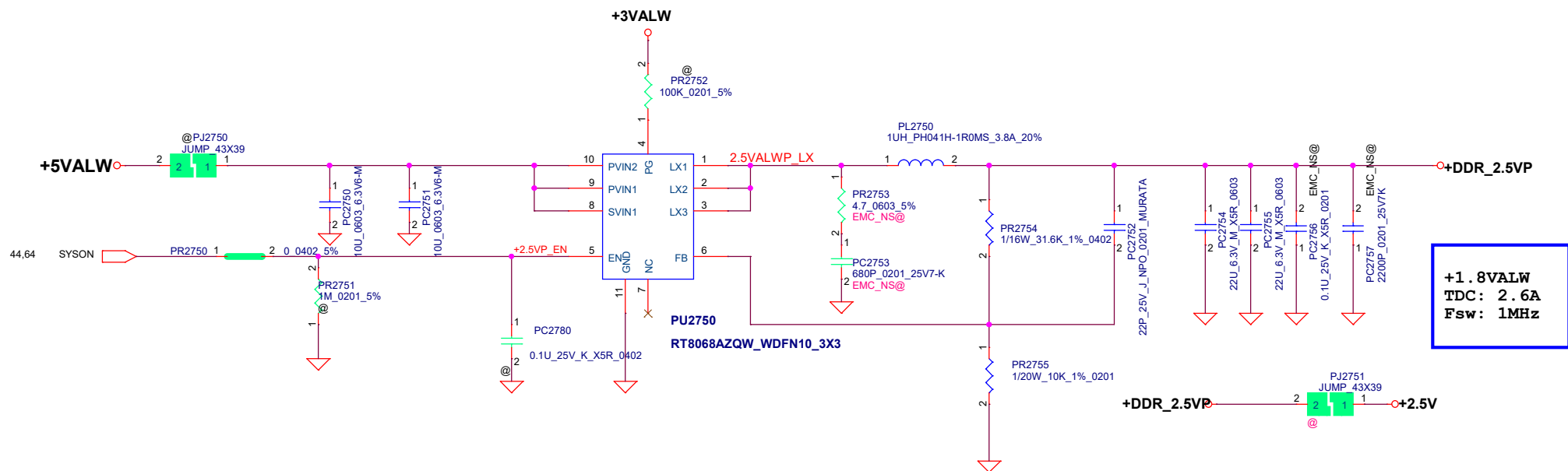


| | | | | | | | | | | | | |
|--|--|------------------------------|--|------------|----|---|--|------|-----------------|--|-----|--|
| Security Classification | | LC Future Center Secret Data | | Title | |  | | | | | | |
| Issued Date | | Deciphered Date | | +0.75VALWP | | | | | | | | |
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| | | | | | | | | 5 | | | 0.2 | |
| Date: | | Tuesday, January 26, 2021 | | Sheet | 63 | | | of | 68 | | | |




| STATE | EN1 | EN2 | VDDQ | VTT_REFF | VTT |
|-------|-----|-----|------|----------|------------|
| S0 | Hi | Hi | On | On | On |
| S3 | Lo | Hi | On | On | Off (Hi-Z) |
| S4/S5 | Lo | Lo | Off | Off | Off |

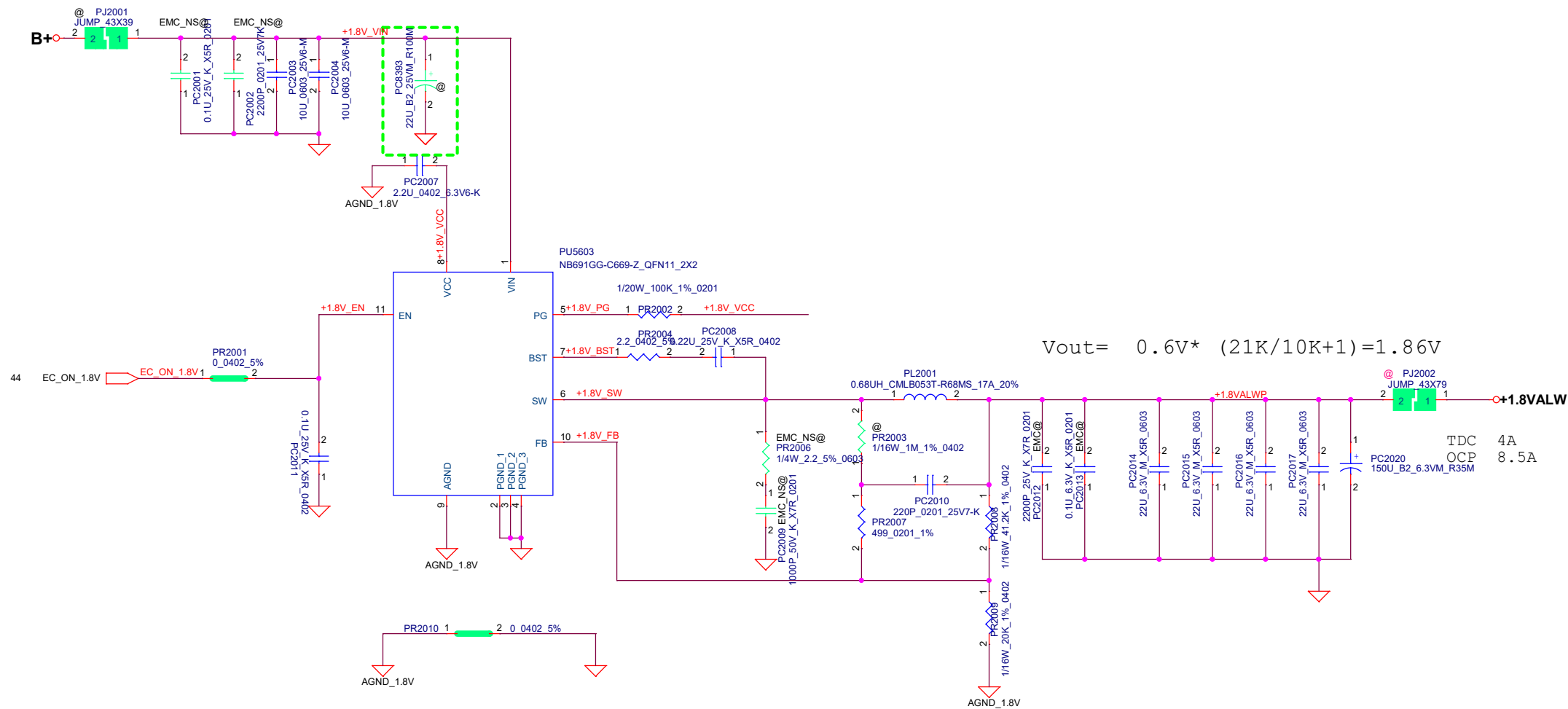
Note: S3 - sleep; S5 - power off



VREF = 0.6V

$V_{out} = 0.6 * (1 + 162k / 51K) = 2.506V$

| | | | | | | |
|--|---------------------------|------------------------------|-------|---------------------|-------|---|
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| Issued Date | | Deciphered Date | | | | |
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| Size | Document Number | | Rev | | 0.2 | |
| Date: | Tuesday, January 26, 2021 | | Sheet | 65 | of 68 | |



| | | |
|----------|--------------------------------|----------------|
| Title | | |
| +1.8VALW | | |
| Size B | Document Number Drift AMD 3 | Rev 0.2 |
| Date: | Tuesday, January 26, 2021 | Sheet 66 of 68 |

